Chapter 6 Cascode Amplifiers

Section 6.1 The Principles behind Cascode Amplifiers

Let us consider the amplifier in Fig. 6.1. This is an ordinary amplifier which is not cascoded. We first perform some experiments so that we can understand how it should be improved.

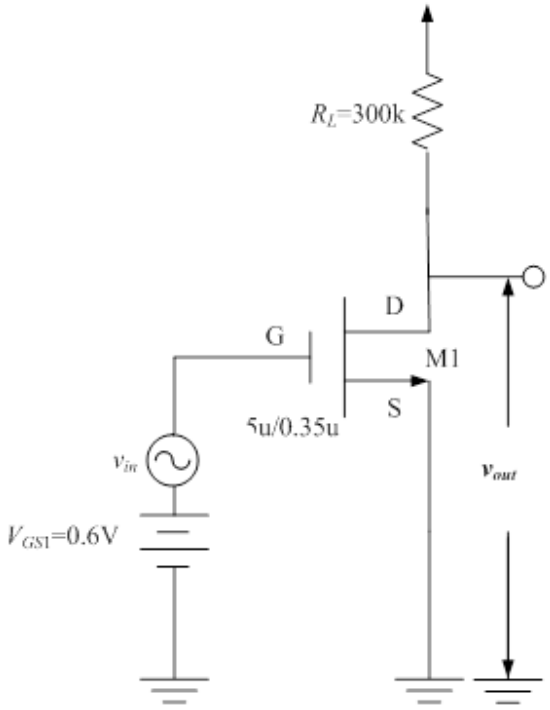


Fig. 6.1-1 An ordinary amplifier

Experiment 6.1-1 The I-V curves and the Load Line of the Amplifier

The program of this experiment is in Table 6.1-1. The result is shown in Fig. 6.1-2. We would like the reader to pay close attention to one problem: The I-V curve of this transistor which is not so flat will definitely affect the gain. In fact, the gain of this amplifier is 35, as expected.

Table 6.1-1 Program for Experiment 6.1-1

```
Ex6.1-1
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post
```

```
VDD      1     0     3.3V
RL   1   11    300k

.param     W1=5u
M1   11    2     0     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG   2     4     0.6v
Vin  4     0     0V
VDS        11    0     0V

.DC VDS 0      3.3V 0.1V
.PROBE I(M1) I(RL)
.end
```

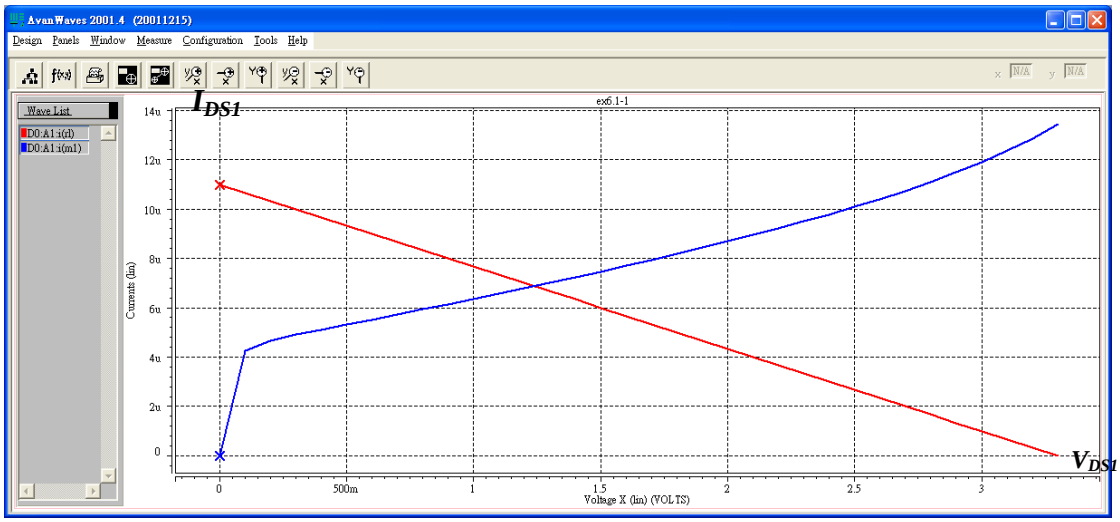


Fig. 6.1-2 The I-V curve and its load line of M1 in Fig 6.1-1

In this section, we should introduce a new kind of amplifier, called the cascode amplifier. Fig. 6.1-3 shows such a typical amplifier. In a cascode amplifier, two NMOS transistors are connected together. One is on top of the other.

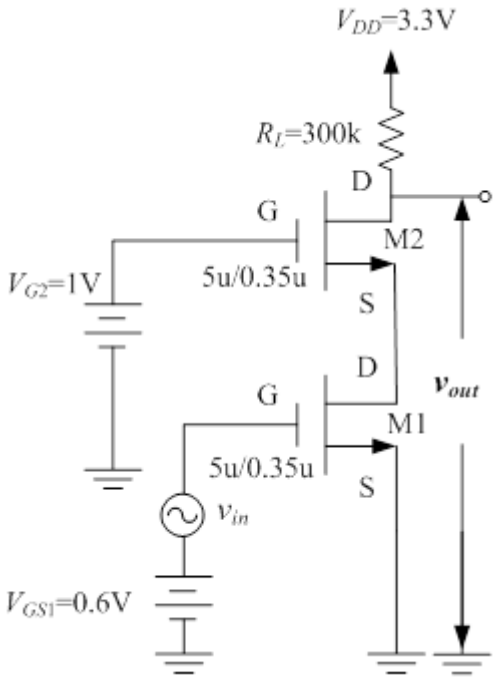


Fig. 6.1-3 A cascade amplifier

The special characteristics of a cascode amplifier is its I-V curve. This can be made clear by the following experiment.

Experiment 6.1-2 The I-V Curve of the Cascode Amplifier in Fig. 6.1-3.

The program of the experiment is in Table 6.1-2. The result is in Fig. 6.1-4. As can be seen, the I-V curve is much flatter. If we compare Fig. 6.1-4 and Fig. 6.1-2, we would find that the current in the cascode amplifier is also much smaller.

Table 6.1-2 Program for Experiment 6.1-2

```
Ex6.1-2
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD     1    0    3.3V
RL      1    11   300k

.param  W1=5u
M2      11   2    3    0
+nch L=0.35u      W='W1' m=1
```

```
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1        3     4     0     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'
VG2       2     0     1v
VGS1      4     6     0.6v
Vin       6     0     0V
Vout      11    0     0V

.DC Vout 0 3.3V 0.1V
.PROBE I(RL) I(M1) I(M2)
.end
```

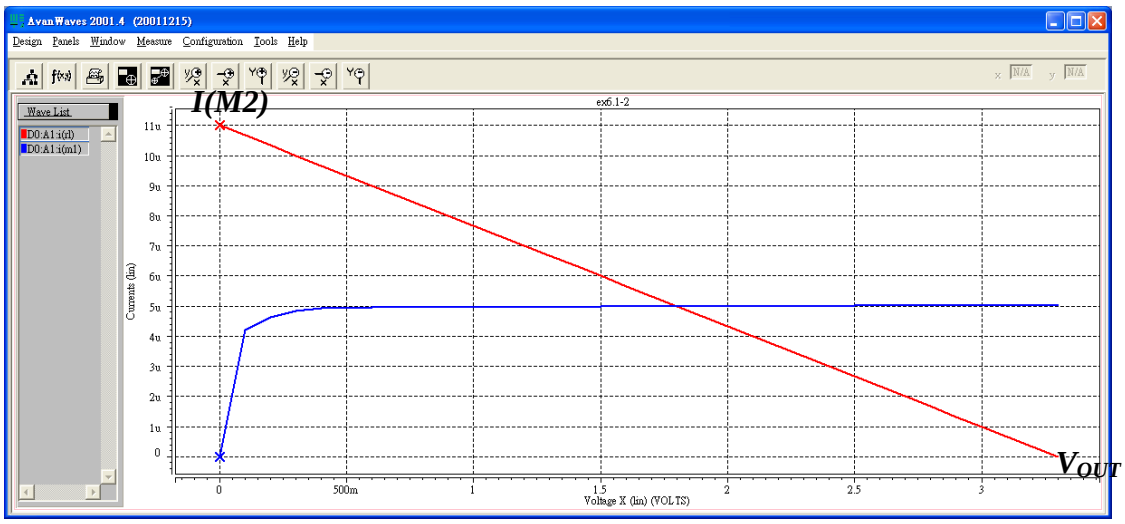
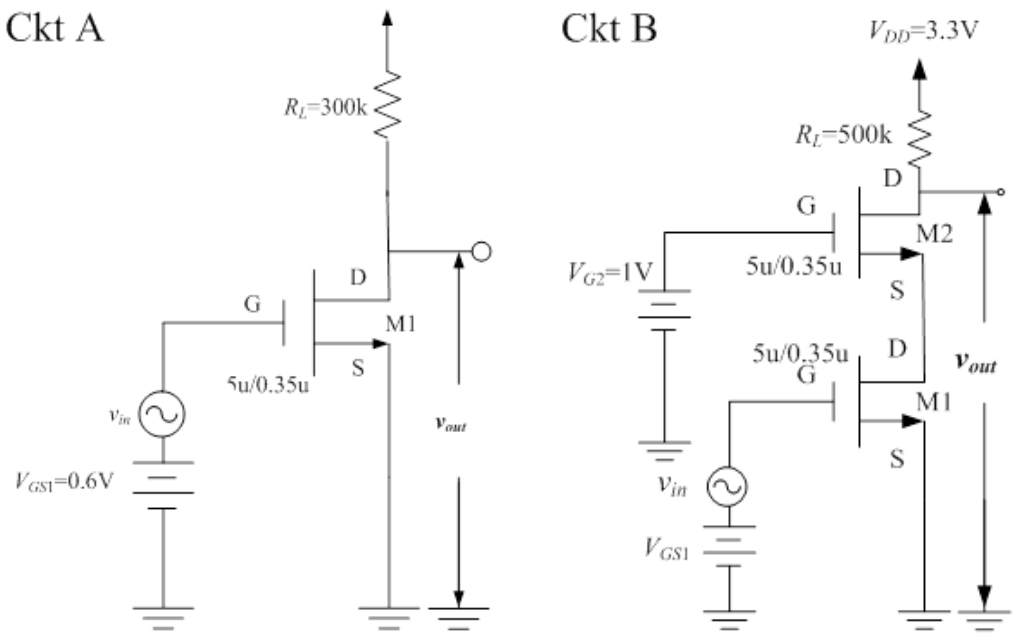


Fig. 6.1-4 The I-V curve of the cascoded transistor

To understand why the I-V curve is much flatter and its current much smaller in a cascode amplifier, let us redraw a non-cascode amplifier and a cascode amplifier together in Fig. 6.1-5.



(a) A non-cascoded amplifier (b) A cascoded amplifier

Fig. 6.1-5 A non-cascode amplifier and a cascode amplifier

Let us consider the non-saturation region of the non-cascode amplifier, Ckt A. If V_{DS} is increased, current I_{DS} will increase without much constraint until it reaches the saturation region. But, for Ckt B, as we increase V_{DS1}, we face a problem: The increasing of V_{out} will also increase $I_{DS2} = I_{DS1}$. The increasing of I_{DS1} will induce the increasing of V_{DS1}. However, an increasing of V_{DS1} will decrease V_{GS2}. V_{GS2} cannot be too small because V_{GS2} must be higher than V_{t2}. This implies that V_{DS1} as well as $I_{DS1} = I_{DS2}$ cannot increase very much. That is, as I_{DS1} increases, I_{DS2} will of course increase. But, it will stop increasing earlier than the non-cascoded case, as illustrated in Fig. 6.1-6.

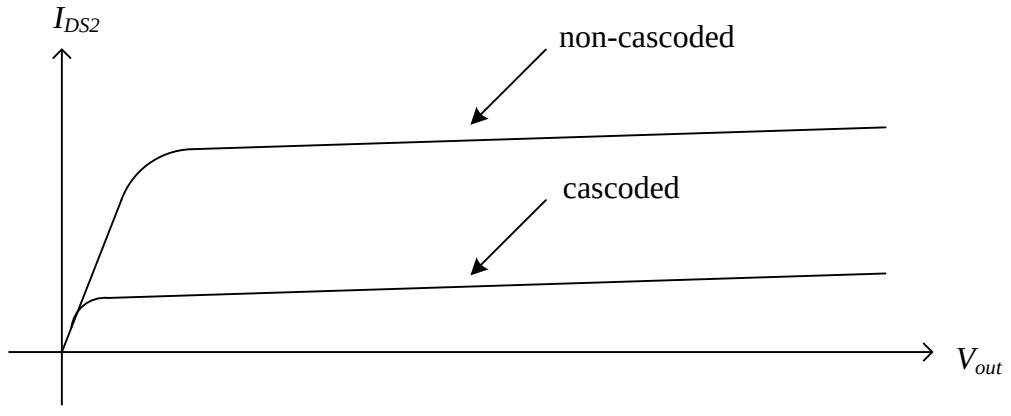


Fig. 6.1-6 The I-V curves of cascoded and non-cascoded transistors

Let us pay attention to V_{DS1} and ask the following questions: Suppose R_L changes, V_{out} will of course change. Will V_{DS1} also change? The answer is "no". Note that I_{DS2} remains the same as long as M2 is in the saturation region. This means that V_{GS2} has to remain roughly the same. Thus V_{DS1} has to be roughly the same because $V_{DS1} = V_{G2} - V_{GS2}$ and V_{G2} is a constant. On the other hand, $V_{out} = V_{DS2} + V_{DS1}$. If V_{out} changes, V_{DS2} may change as V_{DS1} remains unchanged.

Experiment 6.1-3 Comparing the I-V Curves of the Two Amplifiers, the Non-Cascoded and the Cascoded, Shown in Fig. 6.1-5

The program for the cascoded amplifier is shown in Table 6.1-3, that for the non-cascoded one is shown in Table 6.1-4 and the results are shown in Fig. 6.1-7. As can be seen from Fig. 6.1-7, the current in the cascoded amplifier is much smaller than that in the non-cascoded one.

Table 6.1-3 Program for the cascoded amplifier

```
Cascoded Amplifier
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD     1    0    3.3V
RL      1    11   500k

.param  W1=5u
M2      11   2    3    0
+nch L=0.35u      W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1      3    4    0    0
+nch L=0.35u      W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG2     2    0    1v
VGS1    4    6    0v
```

```
Vin         6     0     0
Vout        11    0     0
.DC Vout 0 3.3v 0.1v SWEEP VGS1 0 3.3v 0.1v
.PROBE I(M1) I(M2) I(RL)
.end
```

Table 6.1-4 Program for the non-cascoded amplifier

```
Non-cascode Amplifier
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD         1     0     3.3V
RL          1     11    500k

.param      W1=5u
M1          11    2     0     0
+nch L=0.35u          W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG          2     4     0v
Vin         4     0     0V
VDS1        11    0     0V
.DC VDS1        0     3.3V 0.1V SWEEP VG 0 3.3v 0.1v
.PROBE I(M1) I(RL)
.end
```

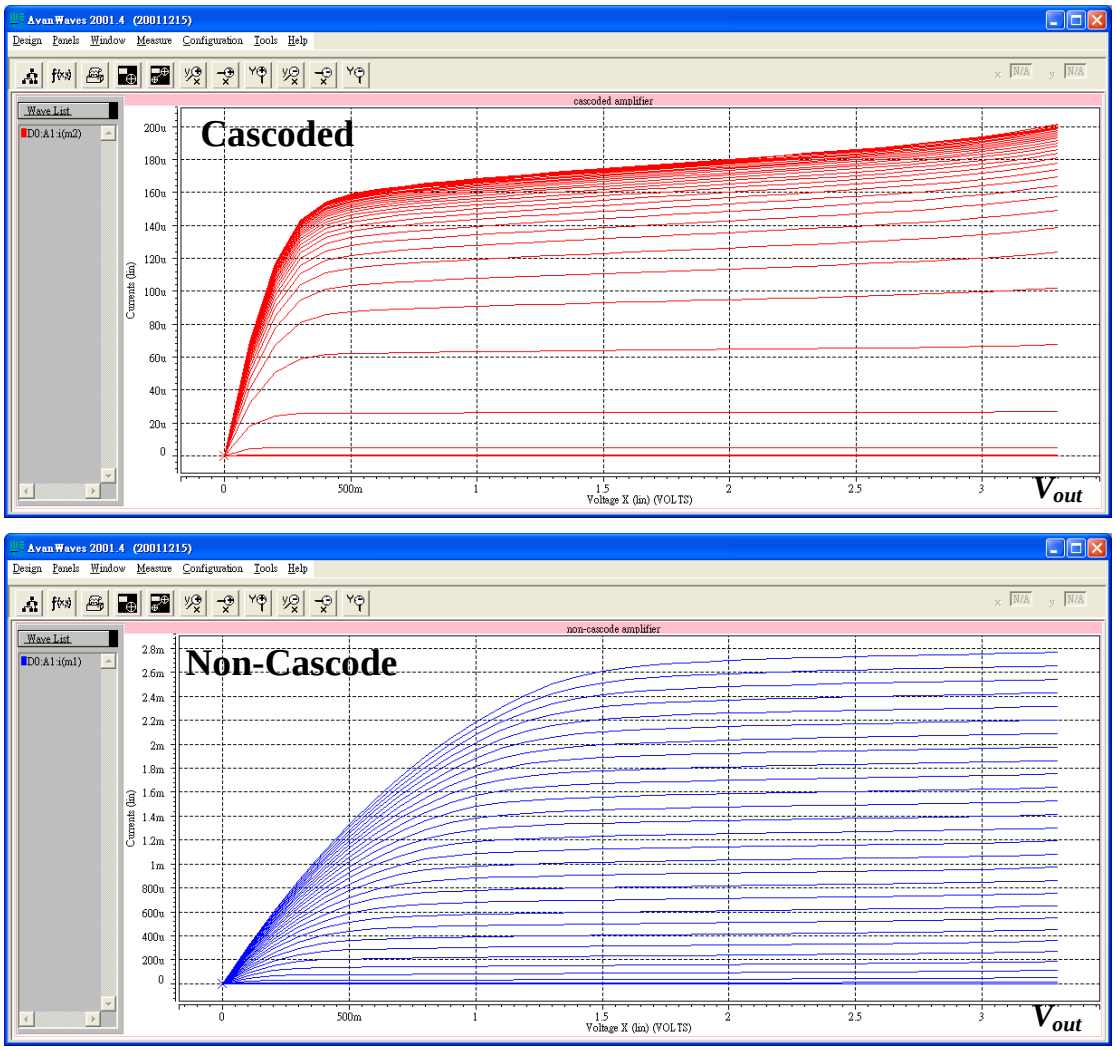


Fig. 6.1-7 I-V curves for cascoded and non-cascoded amplifiers

We may view M2 as a deterrent force to limit the growth of current in M1. Essentially, it is V_{GS2} which plays the trick. If we increase V_{G2}, we shall have a larger current in M2, which is also the current in M1. On the other hand, if we decrease V_{G2}, we shall have an even smaller current in both M2 and M1. This is illustrated in the next experimental result.

Experiment 6.1-4 The Increase of V_{G2}

In this experiment, we first increased V_{G2} from 1V to 2V. This will allow a higher V_{DS1} to grow and the highest current was increased from 0.3ma to 0.9ma. The program is in Table 6.1-5 and the result is shown in Fig. 6.1-8.

Table 6.1-5 Program for Experiment 6.1-4

Ex6.1- 4 Cascoded .protect

```
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD      1     0     3.3V
RL       1     11    500k

.param   W1=5u
M2       11    2     3     0
+nch L=0.35u       W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1       3     4     0     0
+nch L=0.35u       W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG2      2     0     2v
VGS1     4     6     0v

Vin  6     0     0
Vout 11    0     0

.DC Vout 0 3.3v 0.1v SWEEP VGS1 0 3.3v 0.1v
.PROBE I(M1) I(M2) I(RL)
.end
```

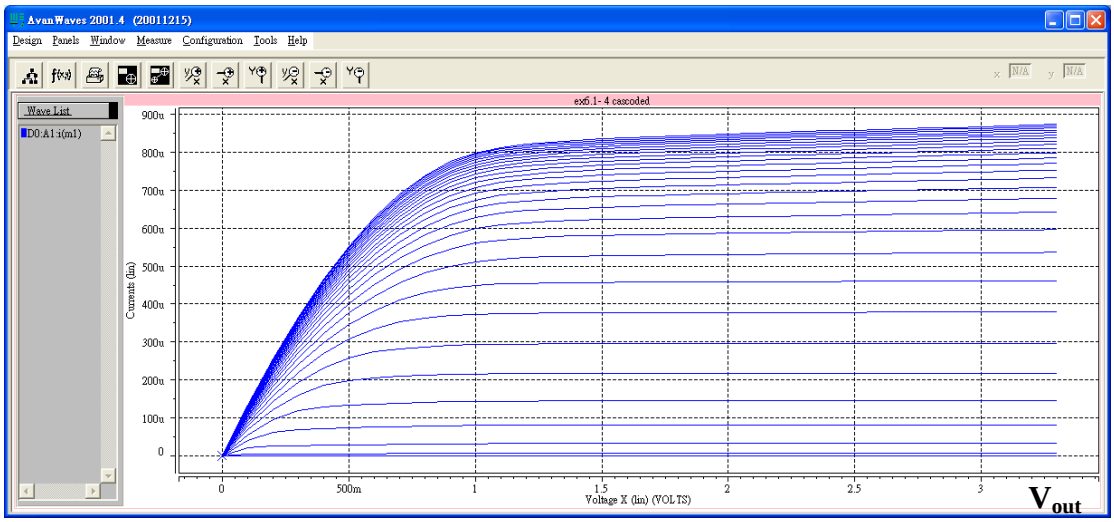


Fig. 6.1-8 The I-V curves for a higher V_{G2}

Experiment 6.1-5 The Decrease of V_{G2}

In this experiment, we reduced V_{G2} from 1V to 0.8V. This will further put a higher constraint for V_{DS1} to grow and the highest current was decreased from 0.3mA to 0.09mA, as shown in Fig. 6.1-9. The program is shown in Table 6.1-6.

Table 6.1-6 Program for Experiment 6.1-5

```
Ex6.1-5 Cascoded
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD      1    0    3.3V
RL       1    11   500k

.param   W1=5u
M2       11   2    3    0
+nch L=0.35u       W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1       3    4    0    0
+nch L=0.35u       W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
```

```
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG2      2    0    0.8v
VGS1     4    6    0v

Vin      6    0    0
Vout     11   0    0

.DC Vout 0 3.3v 0.1v SWEEP VGS1 0 3.3v 0.1v
.PROBE I(M1) I(M2) I(RL)
.end
```

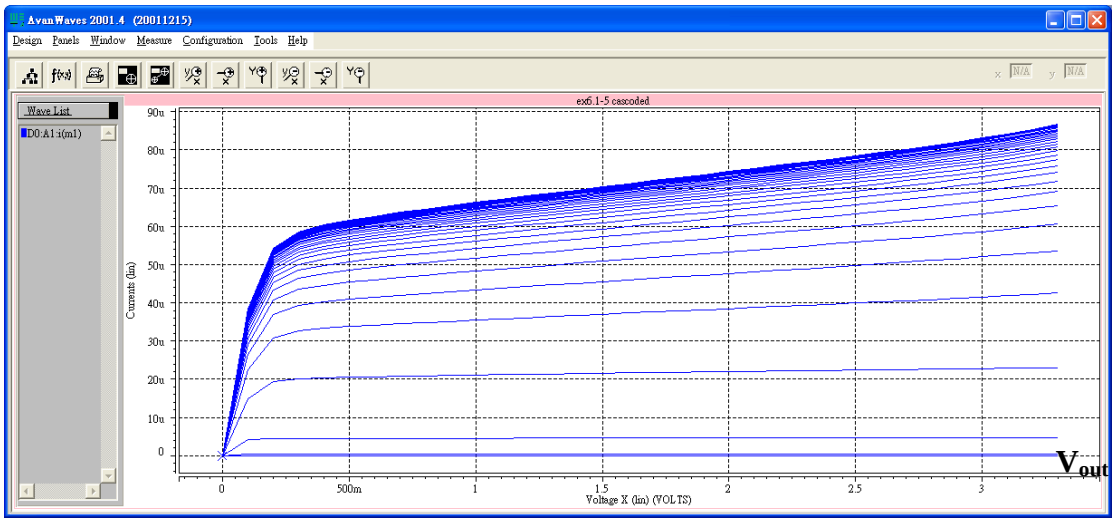
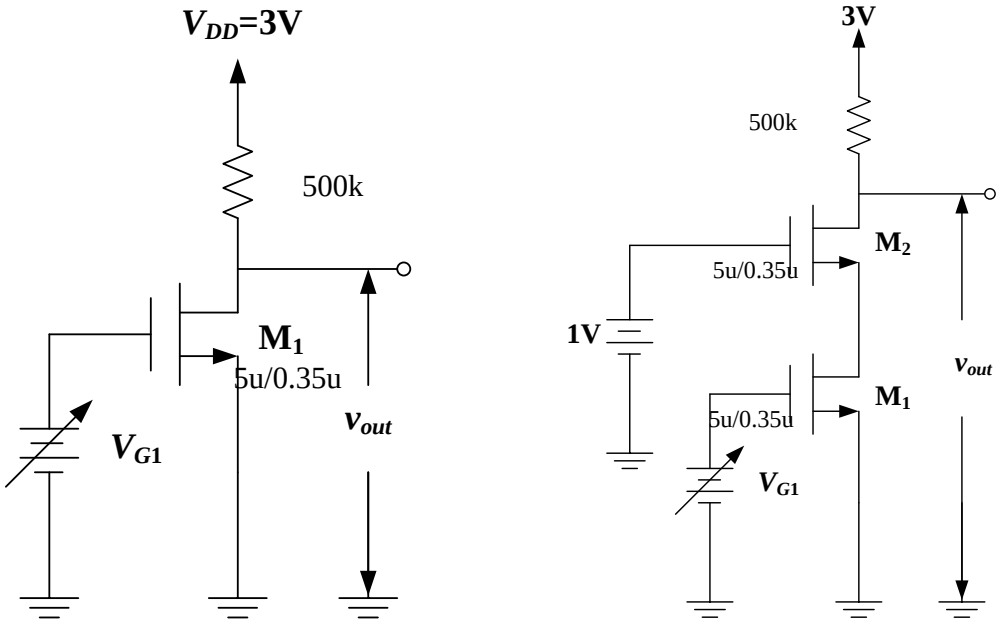


Fig. 6.1-9 The I-V curves for a lower V_{G2}

Experiment 6.1-6 The Comparison of Input/Output Curves for Non-Cascoded Amplifiers and Cascoded Amplifiers

We draw the two amplifiers in Fig. 6.1-10. This experiment is to see the difference between Input/Output curves for non-cascoded and cascoded amplifiers. The program for testing the non-cascoded amplifier is in Table 6.1-7 and its result is in Fig. 6.1-11 The program for testing the cascoded amplifier is in Table 6.1-8 and the result is in Fig. 6.1-12. We can see that the input-output is much shaper for the cascode amplifier than that for the non-cascoded amplifier.



(a) A non-cascoded amplifier (b) A cascoded amplifier

Fig. 6.1-10 Amplifier for Experiment 6.1-6

Table 6.1-7 Program to obtain the Input/Output corves for the non-cascoded amplifier

```
Example 6.1-6 Non-Cascode Case
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD      1     0     3.3V
RL   1     11    500k

.param     W1=5u
M1   11    2     0     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG   2     0     0
.DC VG 0 3.3v 0.1v
.end
```

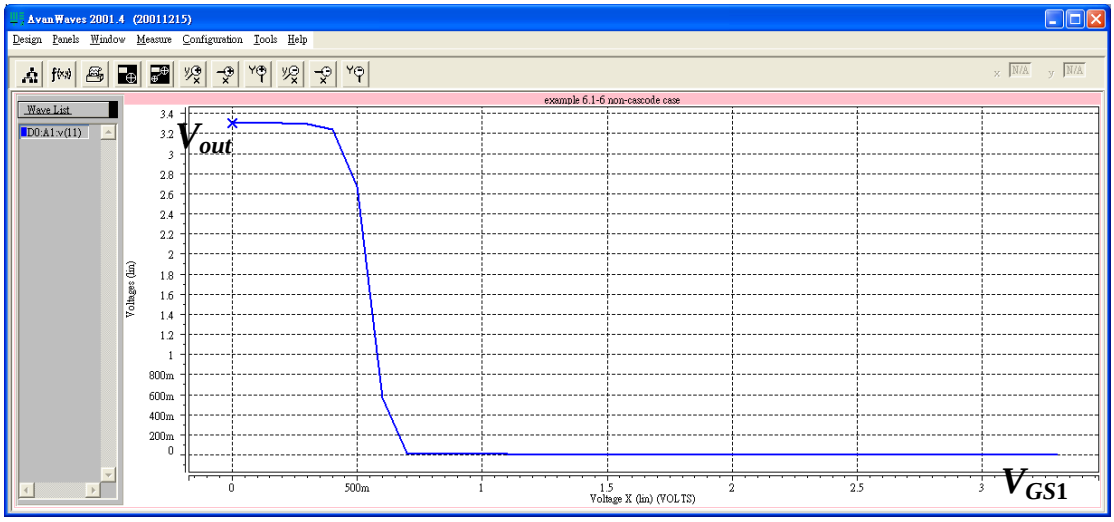


Fig. 6.1-11 The input/output curve of the non-cascoded amplifier

Table 6.1-8 Program to obtain the V_{GS1}/V_{out} curve for the cascoded amplifier

```
Example 6.1-6 Cascode Case
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD      1     0     3.3V
RL   1     11    500k

.param     W1=5u
M2   11    2     3     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1   3     4     0     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG2       2     0     1v
VGS1      4     0     0
```

```
.DC VGS1 0 3.3v 0.1v
.end
```

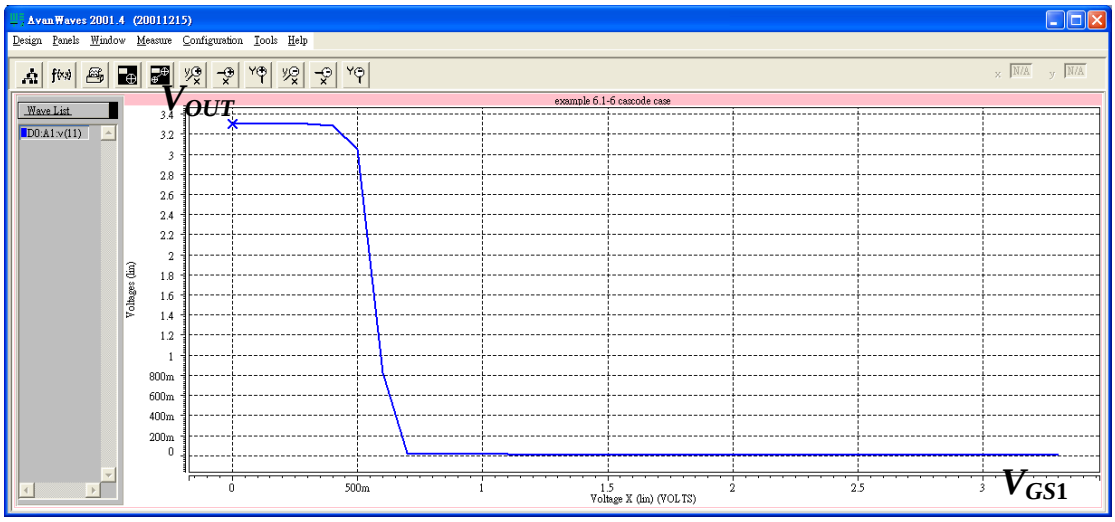


Fig. 6.1-12 The input/output of the cascoded amplifier

Experiment 6.1-7 The Changing of V_{DS2}, V_{DS1} and I_{DS1} as R_L Changes

In this experiment, we increased R_L from 100k to 500k. The purpose was to examine how V_{DS2}, V_{DS1} and I_{DS1} change when R_L is increased. As expected, I_{DS1} will not change much because M2 is in the saturation region. V_{GS2} cannot change much because I_{DS2} is almost a constant. Therefore, V_{DS1} will not change much because $V_{DS1} = V_{G2} - V_{GS2}$. Since V_{out} decreases as R_L increases, V_{DS2} decreases. The program is shown in Table 6.1-9. The result is shown in Table 6.1-10.

Table 6.1-9 Program for Experiment 6.1-7

```
Example 6.1-7
.PROTECT
.OPTION POST
.LIB 'c:\mm0355v.l' TT
.UNPROTECT
.op

VDD      1     0     3.3V
RL   1     11    500k

.param     W1=5u
```

```
M2  11    2     3     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1  3     4     0     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'
VG2       2     0     1v
VGS1      4     0     0.6v

.PROBE    I(RL)    I(M2)
.end
```

Table 6.1-10 The parameters of the cascoded mplifier with respect to the change of R_L

RL	VDS2	VDS1	IDS1
100k	2.445V	0.351V	5.014u
200k	1.954V	0.344V	4.999u
300k	1.466V	0.337V	4.985u
400k	0.981V	0.330V	4.969u
500k	0.499V	0.323V	4.954u

Experiment 6.1-8 The Changing of V_{out} with Respect to the Changing of R_L

In this experiment, we tried to see how the decreasing of R_L will affect V_{out}. The program is in Table 6.1-11 and the result is in Fig. 6.1-13.

Table 6.1-11 Program for Experiment 6.1-8

```
Example 6.1-8
.PROTECT
```

```
.OPTION POST
.LIB 'c:\mm0355v.l' TT
.UNPROTECT
.op

VDD      1     0     3.3V
RL   1     11    XVAL

.param     W1=5u
M2   11    2     3     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1   3     4     0     0
+nch L=0.35u         W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'
VG2       2     0     1v
VGS1      4     0     0.6v
Vout 11    0     0V

.DC Vout    0 3.3V 0.1V  SWEEP   XVAL      100k       500k       100k
.PROBE    I(RL)    I(M2)
.end
```

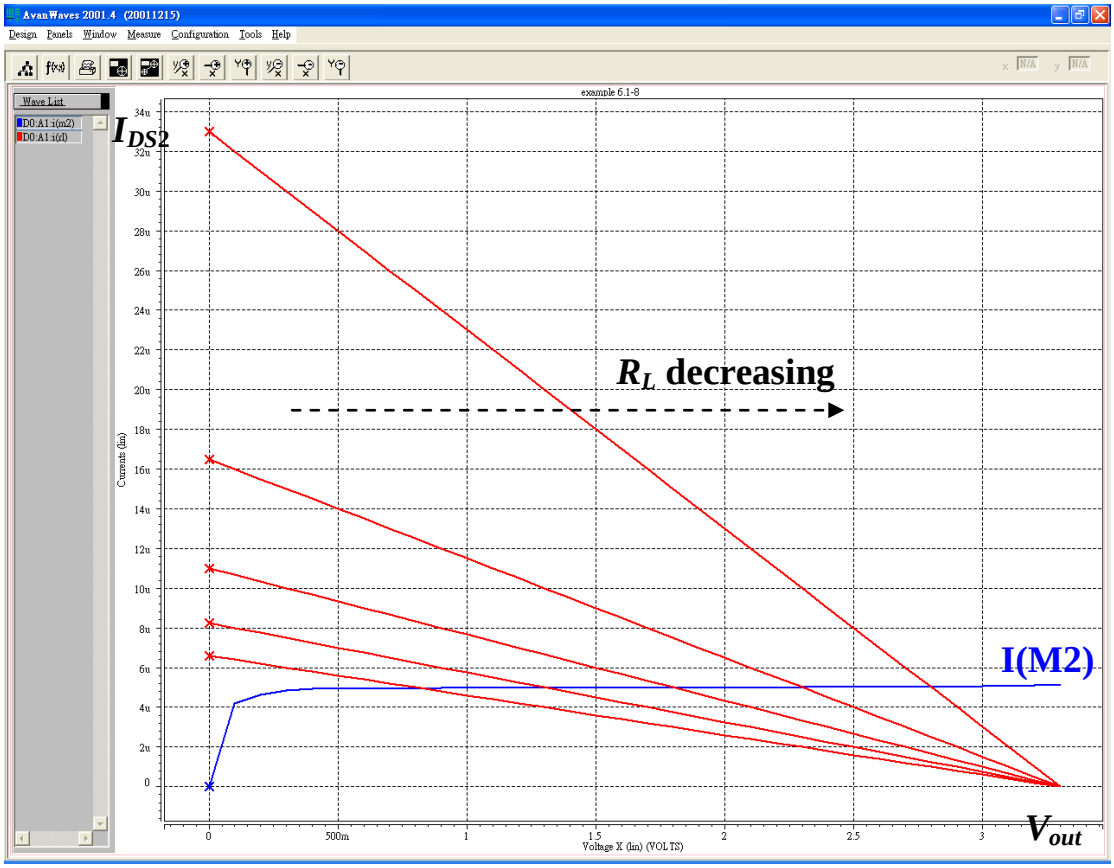


Fig. 6.1-13 The changing of V_{out} with respect to the changing of R_L

Experiment 6.1-9 The Changing of V_{DS1} with Respect to the Changing of R_L

As we indicated before, V_{DS1} will not change as R_L changes. This experiment shows this point. The program is in Table 6.1-12 and the result is in Fig. 6.1-14. Note that the increase of V_{DS1} causes a decrease of V_{GS2}. We should also note that when $V_{DS1} = 0.5V$, $V_{GS2} = (1-0.5)V = 0.5V$ and the current drops to zero as M_2 is cut off.

Table 6.1-12 Program for Experiment 6.1-9

```
Example 6.1-9
.PROTECT
.OPTION POST
.LIB 'c:\mm0355v.l' TT
.UNPROTECT
.op

VDD     1     0     3.3V
RL  1     11    XVAL
```

```
Rv   3     9     0

.param     W1=5u
M2   11    2     3     0
+nch L=0.35u        W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1   9     4     0     0
+nch L=0.35u        W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'
VG2        2     0     1v
VGS1       4     0     0.6v
VDS1       9     0     0V

.DC VDS1    0 3.3V 0.1V      SWEEP   XVAL     100k       500k       100k
.PROBE    I(M1)    I(Rv)
.end
```

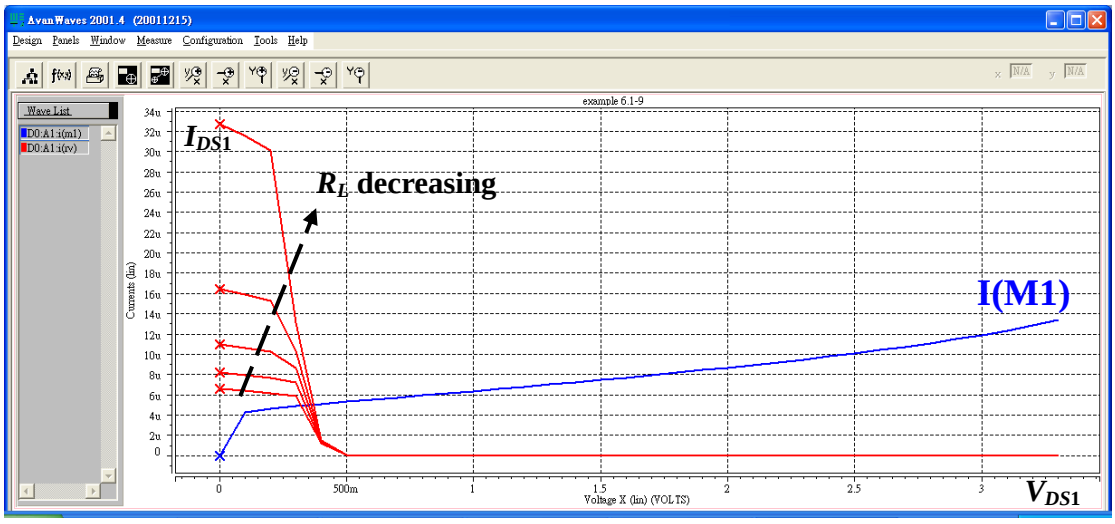


Fig. 6.1-14 I_{DS1} vs V_{out} for the cascoded amplifier

Experiment 6.1-10: The testing of the characteristics of a cascaded transistor

We like to remind the reader that a cascaded transistor is still a transistor. It has its own IV curve. In this experiment, we try to find out the characteristics of a cascaded transistor. This transistor is the one in Fig. 6.1-3. The program is in

Table 6.1-10.

Table 6.1-10 The program of Experiment 6.1-10

```
Example 6.1-10
.PROTECT
.OPTION POST
.lib 'D:\model\tsmc\MIXED035\mm0355v.l' TT
.unprotect
.op
.options nomod post



VDD      1     0     3.3V
RL       1     11    500k
.param   W1=5u
M2       11    2     3     0
+nch L=0.35u       W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

M1       3     4     0     0
+nch L=0.35u       W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

VG2      2     0     1v
VGS1     4     6     0.6v

Vin      6     0     0
Vout     11    0     0
.DC Vout 0 3.3v 0.1v
.PROBE I(M1) I(M2) I(RL) I(rm)
.
end
```

Fig. 6.1-15 shows the IV curve of the cascaded transistor.

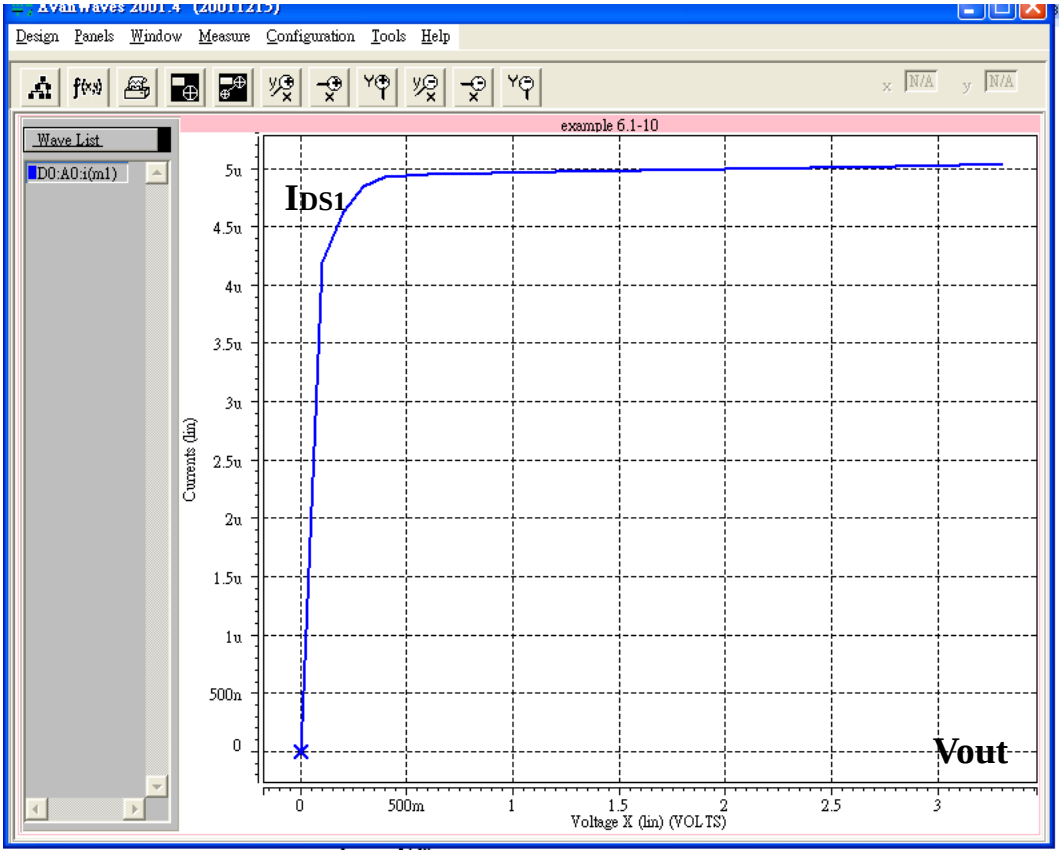


Fig. 6.1-15 The IV curve of the transistor when VG2=1V

We further investigated V_{DS1} and V_{DS2} vs Vout. The result is in Fig. 6.1-16. Note that the current of the cascaded transistor is basically constant quickly after Vout is high enough as shown in Fig. 6.1-15. Therefore V_{GS2} must be a constant. Since V_{G2} is a constant, $V_{S2}=V_{D1}$ must be a constant. Therefore V_{DS1} is a constant. As for V_{DS2}, since Vout increases all the way, $V_{DS2}=Vout-V_{S2}=Vout-V_{D1}$ is increasing.

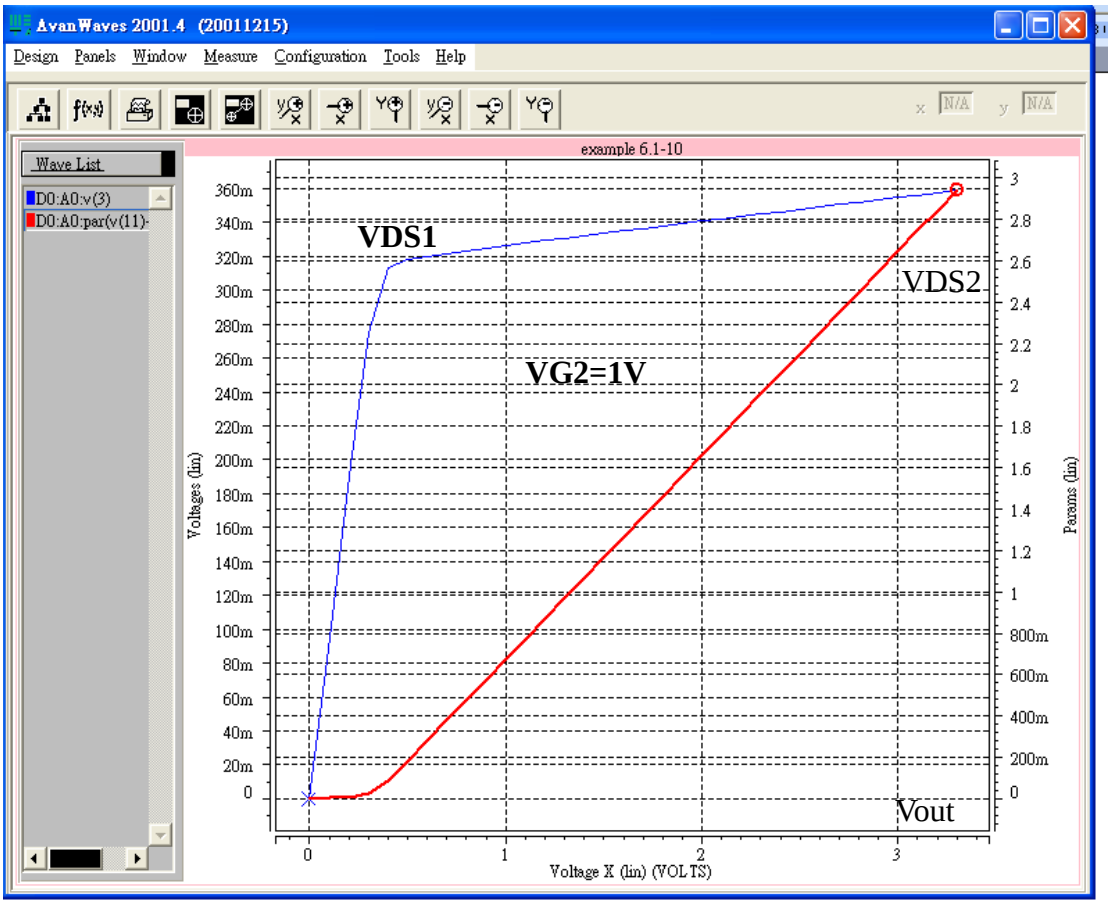
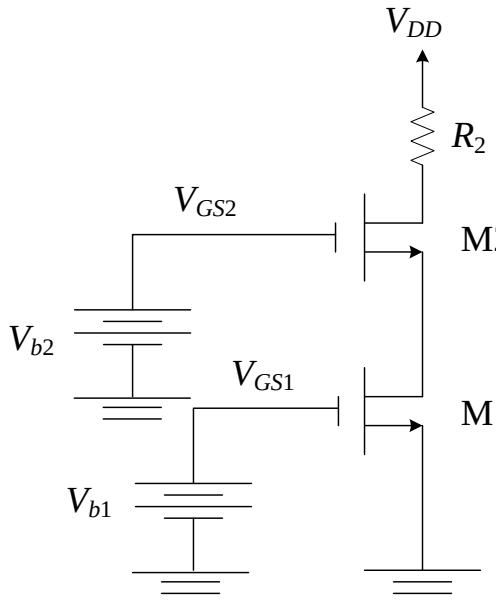


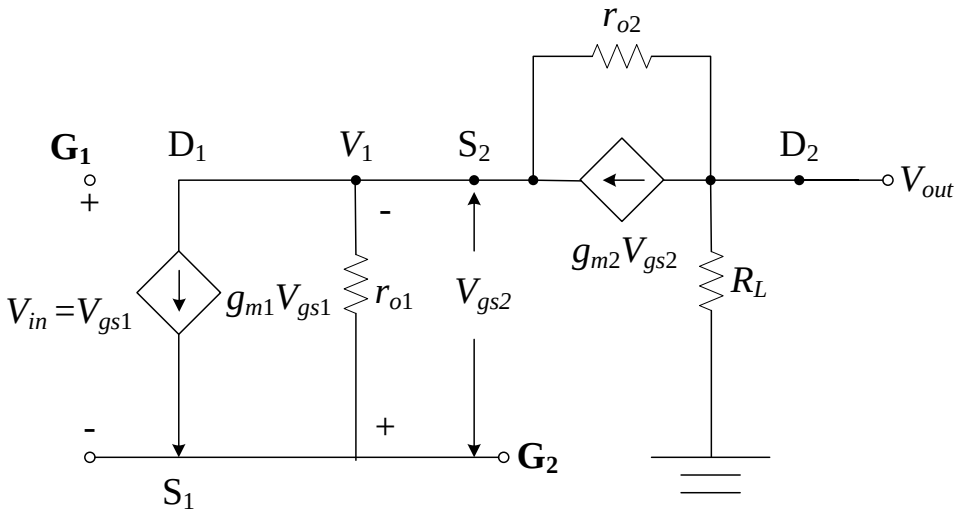
Fig. 6.1-16 V_{DS1} and V vs Vout

Section 6.2 The AC Small Signal Analysis of Cascode Amplifiers

Let us consider the cascoded amplifier in Fig. 6.2-1(a). Its small signal equivalent circuit is in Fig. 6.2-1(b).



(a) A cascoded amplifier



(b) The small signal equivalent circuit for the cascoded amplifier

Fig. 6.2-1 The AC analysis of the cascoded amplifier

We perform node analysis at various nodes.

At S_2:

$$\frac{v_1}{r_{o1}} + \frac{v_1 - v_{out}}{r_{o2}} + g_{m1} v_{gs1} = g_{m2} v_{gs2}$$

Furthermore, as seen in Fig. 6.2-1(b),

$$v_{gs2} = -v_1$$

Besides, $v_{gs1} = v_{in}$. Thus,

$$\frac{v_1}{r_{o1}} + \frac{v_1 - v_{out}}{r_{o2}} + g_{m1} v_{in} = -g_{m2} v_1$$

$$v_1 \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2} \right) - \frac{v_{out}}{r_{o2}} = -g_{m1} v_{in} \qquad (6.2\text{-}1)$$

At D_2:

$$\frac{v_1 - v_{out}}{r_{o2}} = g_{m2} v_{gs2} + \frac{v_{out}}{R_L}$$

Again, $v_{gs2} = -v_1$. Thus we have

$$v_1 \left(\frac{1}{r_{o2}} + g_{m2} \right) = v_{out} \left(\frac{1}{r_{o2}} + \frac{1}{R_L} \right) \qquad (6.2\text{-}2)$$

From (6.2-1) and (6.2-2), we have:

$$\frac{v_{out}}{v_1} = \frac{R_L (1 + g_{m2} r_{o2})}{r_{o2} + R_L} \qquad (6.2\text{-}3)$$

$$\frac{v_{out}}{v_{in}} = \frac{-g_m r_{o1} (1 + g_{m2} r_{02}) R_L}{r_{01} (1 + g_{m2} r_{o2}) + r_{o2} + R_L} \qquad (6.2\text{-}4)$$

Let us assume that $R_L \approx r_{o2}$. Then

$$\frac{v_{out}}{v_{in}} = -g_{m2} r_{o2} \tag{6.2-5}$$

Since r_{o2} is quite large because of the cascoding, we expect a rather high gain from Equation (6.2-5). Note that we obtain this result under the assumption that the load resistor is very large. A large resistor can now be used because the current in the transistors is very low. The reader is encouraged to consult Fig. 6.1-4. The I-V curve is flat and the current is low. A large resistor can thus be used. But it is not a practical idea because a large resistor can hardly be implemented in a VLSI chip.

In the next section, we shall introduce cascoded amplifiers with active loads. As can be imagined, the gain is much higher.

Section 6.3 A Cascoded Amplifier with Active Loads

Consider Fig. 6.3-1. The circuit is a cascoded amplifier with active loads. The purpose of the active load is to provide an even higher load so that we will achieve a higher gain.

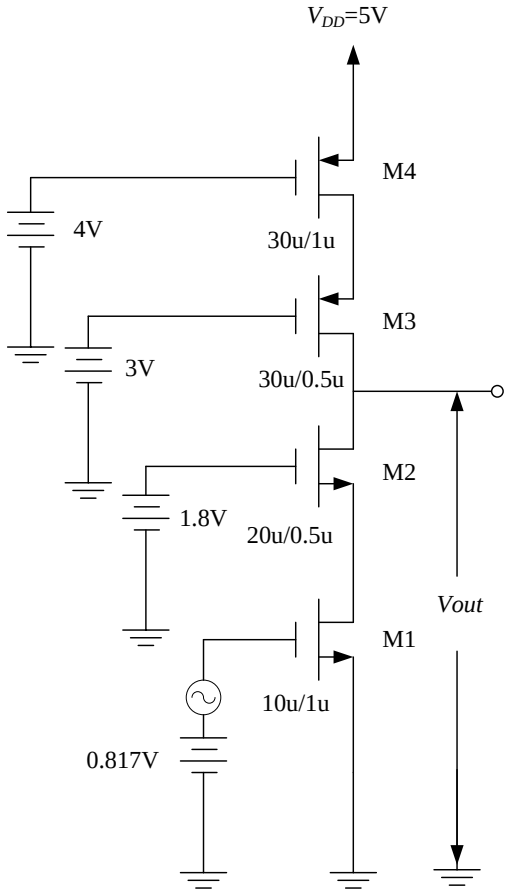


Fig. 6.3-1 A cascoded amplifier with active loads

Experiment 6.3-1 I-V Curve and the Load Line of M2 in Fig. 6.3-1.

In this experiment, we shall try to see the I-V curve and the load curve of M2 in the circuit in Fig. 6.3-1. The program is in Table 6.3-1 and the result is in Fig. 6.3-2.

Table 6.3-1 Program for Experiment 6.3-1

```
Ex6.3-1
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
```

```
.options nomod post

VDD             1           0           5V
Rm3       vout       vout_1    0
Rm1       1          1_1       0

.param    W1=10u W2=20u W3=30u W4=30u

M4        3          2          1_1        1
+pch L=1u      W='W4' m=1
+AD='0.95u*W4' PD='2*(0.95u+W4)'
+AS='0.95u*W4' PS='2*(0.95u+W4)'

M3        vout       4          3          1
+pch L=0.5u    W='W3' m=1
+AD='0.95u*W3' PD='2*(0.95u+W3)'
+AS='0.95u*W3' PS='2*(0.95u+W3)'

M2        vout_1     6          7          0
+nch L=0.5u    W='W2' m=1
+AD='0.95u*W2' PD='2*(0.95u+W2)'
+AS='0.95u*W2' PS='2*(0.95u+W2)'

M1  7     8     0     0
+nch L=1u      W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

Vin  8     9     0
VG19      0     0.817V
VG26      0     1.8V
VG34      0     3V
VG42      0     4V

Vout vout_1     0     0
.DC Vout 0 5v 0.1v
.PROBE I(M2) I(Rm3)
.end
```

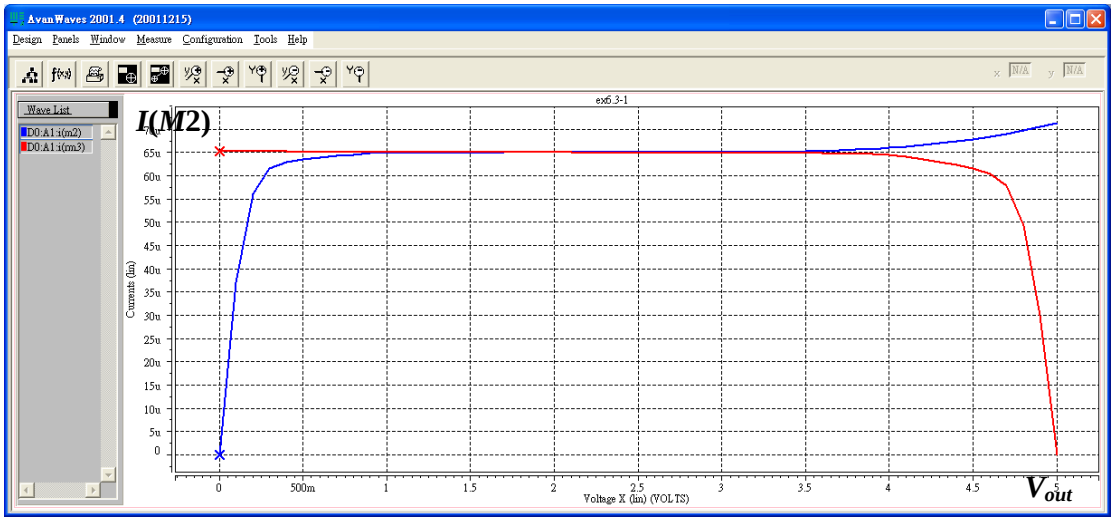


Fig. 6.3-2 The matching of the I-V curve of M2 with its load curve

Fig. 6.3-2 shows that the load curve is very flat and the load curve, which is the I-V curve of M3, is also very flat. We may say that the r_o of M2 almost matches exactly with the r_o of M3. This cannot be achieved with a resistive load.

Experiment 6.3-2 The V_{GS1} and V_{out} Relationship of the Cascoded Amplifier in Fig. 6.3-1

We further drew the V_{GS1} vs V_{out} curve. The program is in Table 6.3-2 and the result is in Fig. 6.3-3. We can now see that the V_{out} drops sharply and thus will induce a very high gain, as confirmed in the next experiment.

Table 6.3-2 Program for Experiment 6.3-2

```
Ex6.3-2
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD      1     0     5V
Rm3vout vout_1     0
Rm11     1_1  0

.param     W1=10u W2=20u W3=30u W4=30u
```

```
M4  3     2     1_1  1
+pch L=1u      W='W4' m=1
+AD='0.95u*W4' PD='2*(0.95u+W4)'
+AS='0.95u*W4' PS='2*(0.95u+W4)'

M3  vout 4     3     1
+pch L=0.5u    W='W3' m=1
+AD='0.95u*W3' PD='2*(0.95u+W3)'
+AS='0.95u*W3' PS='2*(0.95u+W3)'

M2  vout_1     6     7     0
+nch L=0.5u    W='W2' m=1
+AD='0.95u*W2' PD='2*(0.95u+W2)'
+AS='0.95u*W2' PS='2*(0.95u+W2)'

M1  7     8     0     0
+nch L=1u      W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

Vin  8     9     0
VG19     0     0V
VG26     0     1.8V
VG34     0     3V
VG42     0     4V

.DC VG1 0 5V 0.1V
.end
```

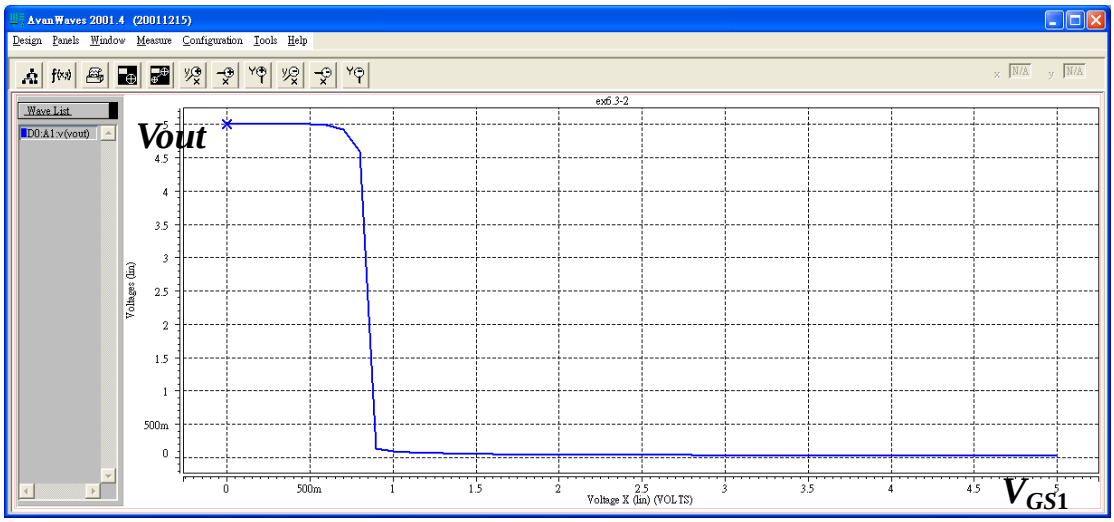


Fig. 6.3-3 V_{out} vs V_{GS1} for the cascoded amplifier in Fig. 6.3-1

Experiment 6.3-3 The Gain of the Cascoded Amplifier in Fig. 6.3-1

The program to find the gain is in Table 6.3-3. The result is shown in Fig. 6.3-4. The gain was found to be 3000.

Table 6.3-3 Program for Experiment 6.3-3

```
Ex6.3-3
.protect
.lib 'c:\mm0355v.l' TT
.unprotect
.op
.options nomod post

VDD      1     0     5V
Rm2vout vout_1     0
Rm11     1_1  0

.param     W1=10u W2=20u W3=30u W4=30u

M4  3     2     1_1  1
+pch L=1u      W='W4' m=1
+AD='0.95u*W4' PD='2*(0.95u+W4)'
+AS='0.95u*W4' PS='2*(0.95u+W4)'

M3  vout 4     3     1
+pch L=0.5u   W='W3' m=1
```

```
+AD='0.95u*W3' PD='2*(0.95u+W3)'
+AS='0.95u*W3' PS='2*(0.95u+W3)'

M2   vout_1     6      7      0
+nch L=0.5u    W='W2' m=1
+AD='0.95u*W2' PD='2*(0.95u+W2)'
+AS='0.95u*W2' PS='2*(0.95u+W2)'

M1   7      8      0      0
+nch L=1u      W='W1' m=1
+AD='0.95u*W1' PD='2*(0.95u+W1)'
+AS='0.95u*W1' PS='2*(0.95u+W1)'

Vin   8      9      sin(0v 0.0001v 10k)
VG19      0      0.817V
VG26      0      1.8V
VG34      0      3V
VG42      0      4V
.tf v(vout) vin
.tran 0.1us 600us
.end
```

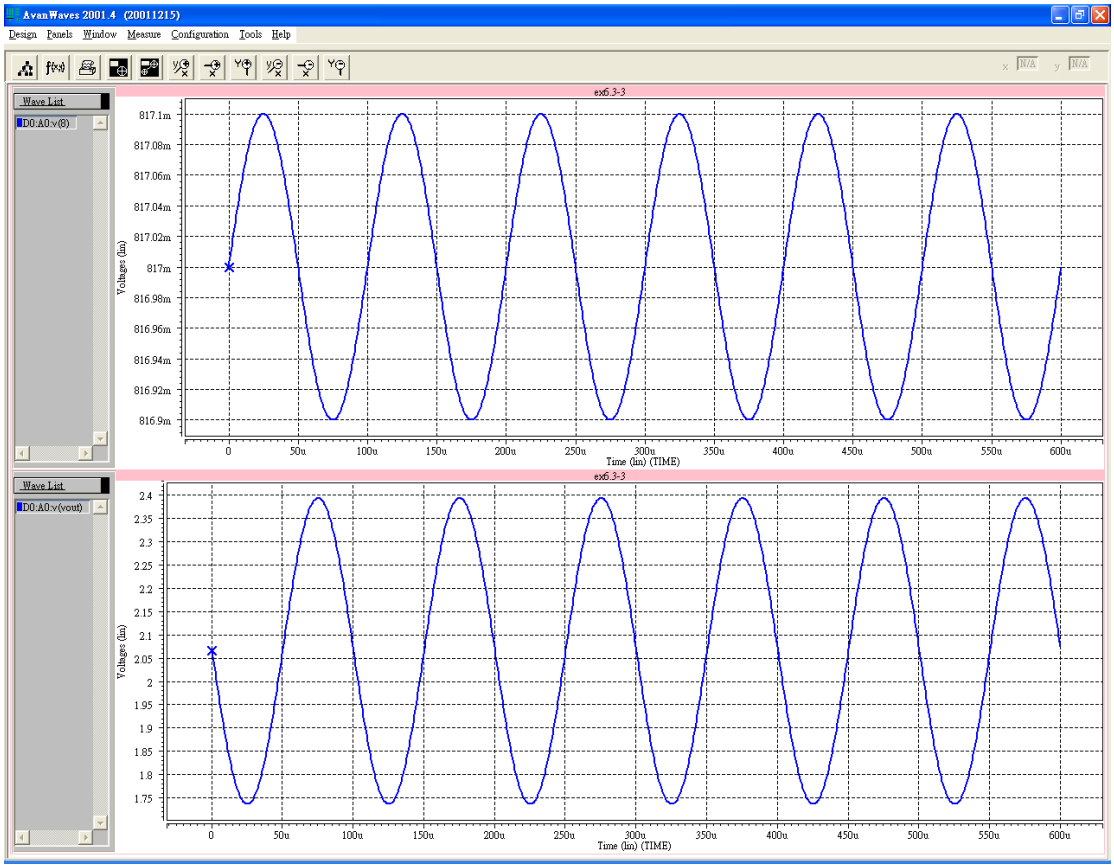


Fig. 6.3-4 The gain of the cascoded amplifier in Fig. 6.3-1

.

Section 6.4 A Cascoded Differential Amplifier

In Fig. 6.4-1, we show a cascoded differential amplifier. This is a two-stage amplifier. The principles of the differential amplifier are the same as that introduced in Chapter 5. It has a high gain because of two mechanisms: the use of the current mirror and the use of the cascoded transistors. The current mirror mechanism would produce a sharp input-output relationship. The cascoding makes the I-V curves very flat which would further make the gain higher.

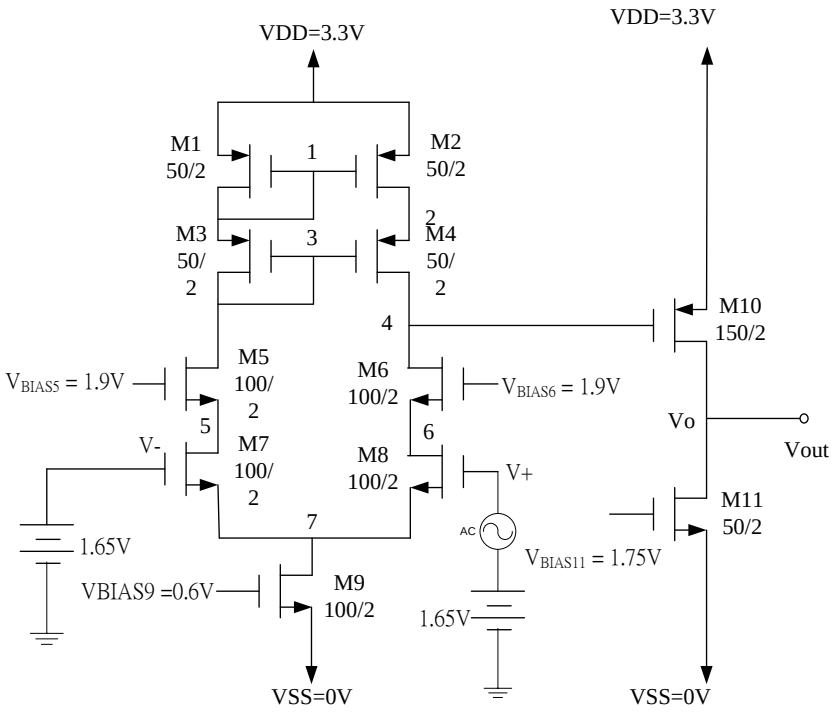


Fig. 6.4-1 A cascoded differential amplifier

Experiment 6.4-1 The Gain of the Cascoded Differential Amplifier Shown in Fig. 6.4-1

The program is in Table 6.4-1 and the result is in Table 6.4-2. The gain was found to be 816.589K, which is very high.

Table 6.4-1 Program for Experiment 6.4-1

```
Experiment 6.4-1
.PROTECT
.OPTION POST
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op
```

```
VDD     VDD!     0     3.3V
VSS VSS!     0     0V

M1  1    1    VDD!   VDD!   PCH    W=50U      L=2U
M2  2    1    VDD!   VDD!   PCH    W=50U      L=2U
M3  3    3    1      VDD!   PCH    W=50U      L=2U
M4  4    3    2      VDD!   PCH    W=50U      L=2U
M5  3    VB7  5      VSS!          NCH        W=100U     L=2U
M6  4    VB8  6      VSS!          NCH        W=100U     L=2U
M7  5    Vi-  7      VSS!          NCH        W=100U     L=2U
M8  6    Vi+  7      VSS!          NCH        W=100U     L=2U
M9  7    VB9  VSS!        VSS!          NCH        W=100U     L=2U
M10 Vo   4    10_1   VDD!   PCH    W=150U     L=2U
M11 Vo   VB11 VSS!        VSS!          NCH        W=50U      L=2U

VIN+     Vi+      0    sin(1.65 0.000001 10k)
VIN-     Vi-  0    1.65
VBIAS7   VB7  0    1.9V
VBIAS8   VB8  0    1.9V
VBIAS9   VB9  0    0.6V
VBIAS11  VB11     0         1.75V

Rm10     VDD!     10_1     0

.tf   V(vo)     vin+
*.tran     1u   10m
.end
```

Table 6.4-2 The gain of the amplifier in Fig. 6.4-1

```
****     small-signal transfer characteristics
    v(vo)/vin+                          =  816.5896k
    input resistance at      vin+       =  1.000e+20
    output resistance at v(vo)          =  8.6934k
```

We also investigate two critrical voltages, namely V4 and V3. V4 and V3 are V_{S4} and V_{S3} respectively. They are shown in Fig. 6.4-2-1. When V+ is small, there will be no current in M8. Therefore, there is no current in M_4 and M_2. But there

will be current in M7. This makes V_{G3} and V_{G1} reasonably large. Thus, the cascoded transistor consisting M_2 and M_4 have large gate voltages, but no current. In such a situation, VDD-V_{S4}=0. This means that V4=V_{S4} very high when V+ is low.

M_7 is sturated when V+ is low. When V+ is low, I(M_7)=I(M_9) and is a constant. Since the cascoded transistor consisting of M_3 and M_1 is a diode now, V3=V_{S3} will be kept as a constant. When V+ reaches 1.65, V4 must be equal to V3. Consequently, it drops sharply at this point.

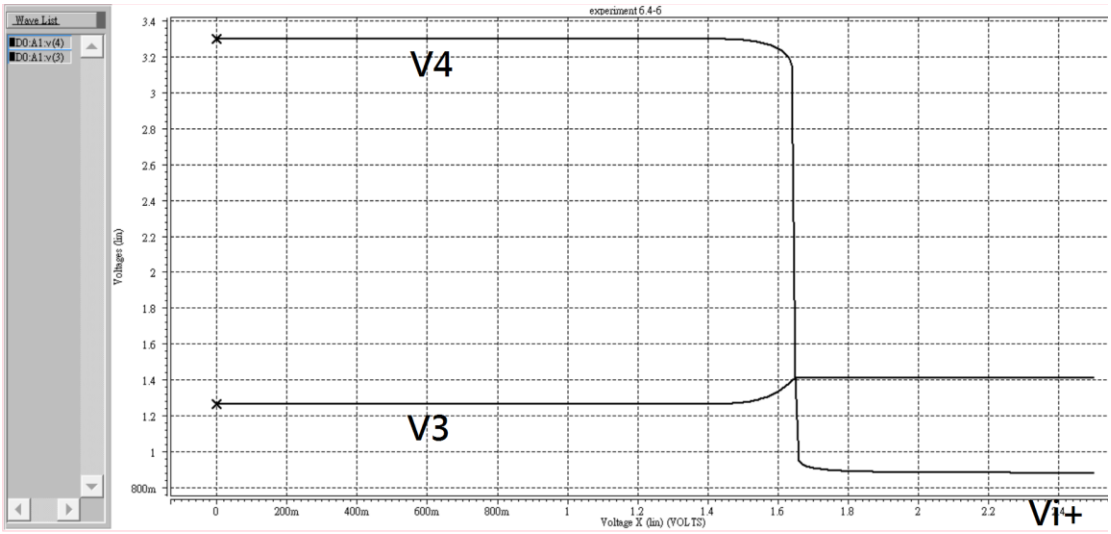


Fig. 6.4-2-1 V4 and V3

Experiment 6.4-2 The V+ versus V_{out} Relationship

The V_+ versus V_{out} Relationship is always important because it is actually the input-output relationship. The program is shown in Table 6.4-3 and the relationship is shown in Fig. 6.4-2. As can be seen, the input/output curve is rather sharp.

Table 6.4-3 Program for Experiment 6.4-2

```
Experiment 6.4-2
.PROTECT
.OPTION POST
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op

VDD     VDD!     0     3.3V
VSS VSS!     0     0V
```

```
M1  1    1    VDD!   VDD!   PCH    W=50U     L=2U
M2  2    1    VDD!   VDD!   PCH    W=50U     L=2U
M3  3    3    1      VDD!   PCH    W=50U     L=2U
M4  4    3    2      VDD!   PCH    W=50U     L=2U
M5  3    VB7  5      VSS!        NCH       W=100U    L=2U
M6  4    VB8  6      VSS!        NCH       W=100U    L=2U
M7  5    Vi-  7      VSS!        NCH       W=100U    L=2U
M8  6    Vi+  7      VSS!        NCH       W=100U    L=2U
M9  7    VB9  VSS!        VSS!        NCH       W=100U    L=2U
M10 Vo   4    10_1   VDD!   PCH    W=150U    L=2U
M11 Vo   VB11 VSS!        VSS!        NCH       W=50U     L=2U

VIN+     Vi+       0    0
VIN-     Vi-  0    1.65
VBIAS7   VB7  0    1.9V
VBIAS8   VB8  0    1.9V
VBIAS9   VB9  0    0.6V
VBIAS11  VB11      0         1.75V

Rm10     VDD!   10_1      0
.DC VIN+      0    3v   0.1v
.end
```

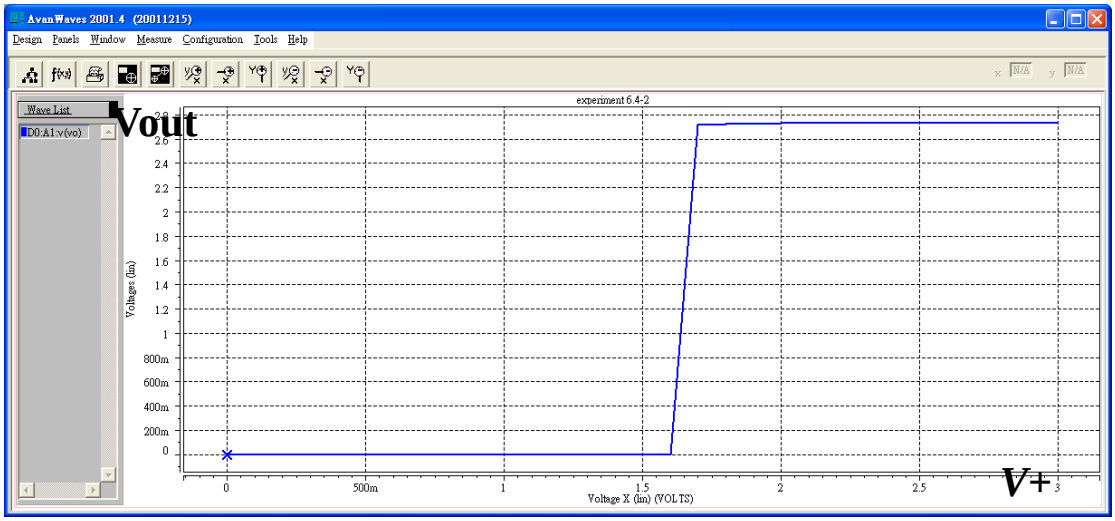


Fig. 6.4-2 V_{out} vs V_{+} for the amplifier in Fig. 6.4-1

Experiment 6.4-3 The I-V Curve of M9 in Fig. 6.4-1 and Its Load Curve

It is perhaps informative to take a look at the I-V curve of M9. The program is in Table 6.4-4 and its load curve is shown in Fig. 6.4-3. We can see that the current in M9 is very small, only 50u. It is this small current which makes its I-V curve very flat and thus its high gain possible.

There is also a load line in Fig. 6.4-3. So, one may ask, what is the load of M9? The answer is: V_{i+} and V_{i-}. As V_{DS9} increases, $V_{GS7} = V_{GS8}$ decreases. Thus the load line shows that the current of M9 decreases. We can also see that by decreasing V_{i+} and V_{i-}, the current of M9 decreases, as expected.

Table 6.4-4 Program for Experiment 6.4-3

```
Experiment 6.4-3
.PROTECT
.OPTION POST
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op

VDD      top      0      3.3V
VSS VSS!      0      0V
R4   44   4    0

M1  1    1          VDD!    VDD!    PCH      W=50U   L=2U
M2  2    1          VDD!    VDD!        PCH      W=50U       L=2U
M3  3    3          1       VDD!        PCH      W=50U       L=2U
M4  44   3          2       VDD!        PCH      W=50U       L=2U
M5  3    VB5        5       VSS!        NCH          W=100U      L=2U
M6  4    VB6        6       VSS!        NCH          W=100U      L=2U
M7  5    Vi-        7       VSS!        NCH          W=100U      L=2U
M8  6    Vi+        7       VSS!        NCH          W=100U      L=2U
M9  7    VB9       VSS!     VSS!        NCH          W=100U      L=2U

VIN+           Vi+        0    1.65
VIN-           Vi-        0    1.65
VBIAS5  VB5       0    1.9V
VBIAS6  VB6       0    1.9V
VBIAS9  VB9       0    0.6V
Vout1      4    0          0

RM9            top        VDD!    0
```

```
VDS9    7          0          0
.DC     VDS9    0 3.3v 0.1v
.probe  I(M9) I(Rm9)
.END
```

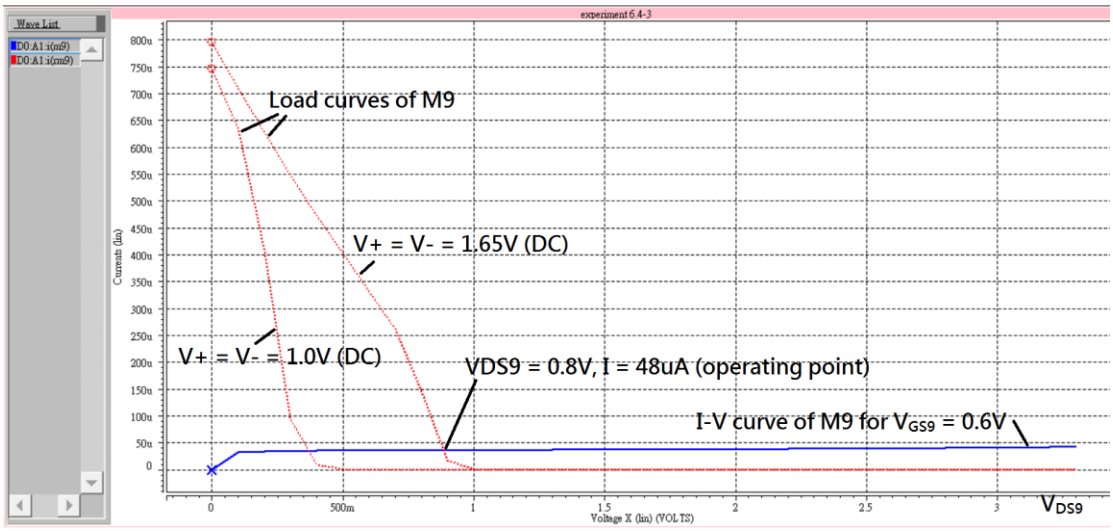


Fig. 6.4-3 The operating points of M9 in Fig. 6.4-1

Experiment 6.4-4 The I-V curve of M10 and its load line.

In this experiment, we show the I-V curve of M10 and its load line. Table 6.4-5 is the program and Fig. 6.4-4 shows the result. As can be seen, the I-V curve of M10 and its load line are not very flat. This is due to the fact that they only a CMOS transistor circuit is used. If a cascaded amplifier is used in the second stage, the gain will be 150 times of that of the present circuit. This gain will be too large.

Table 6.4-5 The program for Experiment 6.4-4

```
Experiment 6.4-1_M10
.PROTECT
.OPTION POST
.LIB “C:\mm0355v.l” TT
.UNPROTECT
.op

VDD      VDD!      0      3.3V
VSS VSS!      0      0V

M1  1     1     VDD!     VDD!     PCH       W=50U         L=2U
```

```
M2  2    1    VDD!   VDD!   PCH    W=50U    L=2U
M3  3    3    1      VDD!   PCH    W=50U    L=2U
M4  4    3    2      VDD!   PCH    W=50U    L=2U
M5  3    VB7  5      VSS!   NCH    W=100U   L=2U
M6  4    VB8  6      VSS!   NCH    W=100U   L=2U
M7  5    Vi-  7      VSS!   NCH    W=100U   L=2U
M8  6    Vi+  7      VSS!   NCH    W=100U   L=2U
M9  7    VB9  VSS!   VSS!   NCH    W=100U   L=2U
M10 Vo   4    10_1   VDD!   PCH    W=150U   L=2U
M11 Vo   VB11 VSS!   VSS!   NCH    W=50U    L=2U

VIN+     Vi+      0    sin(1.65 0.000001 10k)
VIN-     Vi-  0   1.65
VBIAS7   VB7  0   1.9V
VBIAS8   VB8  0   1.9V
VBIAS9   VB9  0   0.6V
VBIAS11  VB11    0        1.75V

Rm10     VDD!   10_1    0
VSD10    VDD!   Vo   0

.DC  VSD10   0    3.3v 0.1v
.probe    I(Rm10)  I(M11)
.end
```

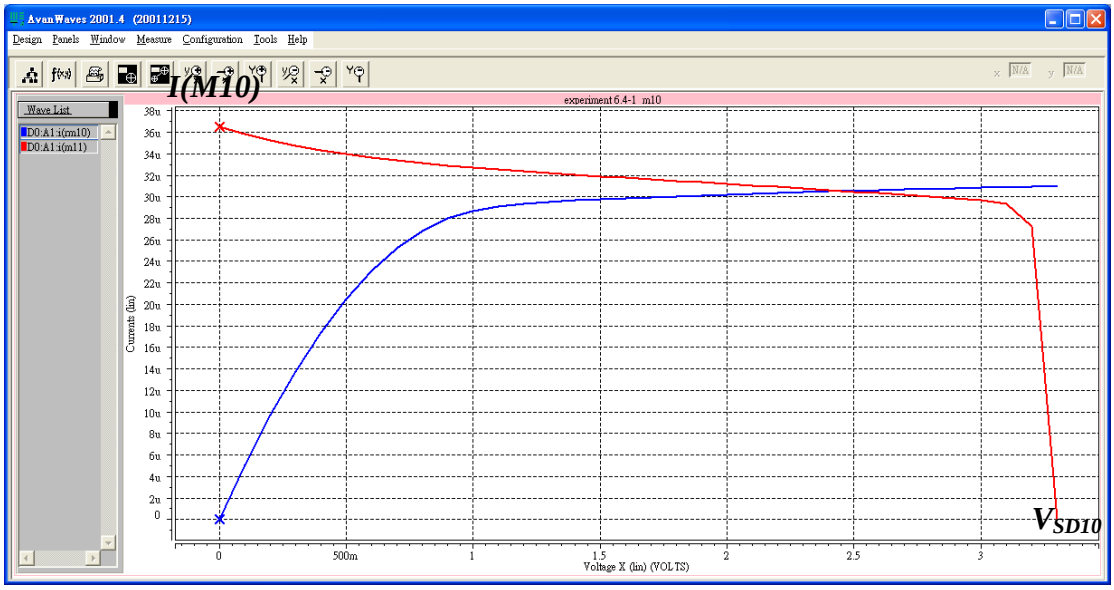


Fig. 6.4-4 The I-V curve of M10 and its load line

In the following example, we shall present an experiment to investigate the voltages and currents of the two-stage cascoded amplifier

Experiment 6.4-5 An investigation into the voltages and currents of the two-stage cascoded amplifier.

Let us first present the circuit as in Fig. 6.4-5 for the simplicity of discussion.

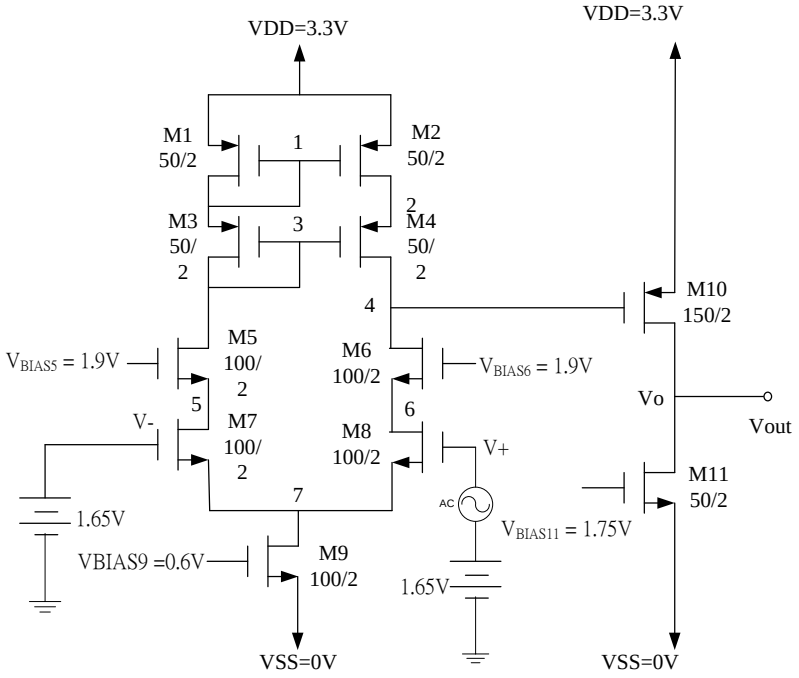


Fig. 6.4-5 The circuit for Experiment 6.4-5.

We first investigate the behavior of currents. The program is shown in Table 6.4-6 and the results are in Fig. 6.4-6. When $V+$ is low, V_{GS8} is low. If V_{GS8} is low, it means that M_4 has a large load and M_4 will be out of saturation region. If M_4 is out of saturation region, the current mirror will not work and $I(M_8) \neq I(M_7)$. As we can see, $I(M_8)$ is zero when $V+$ is low and gradually increases as $V+$ increases. $I(M_7)$ is equal to $I(M_9)$ when $V+$ is low and gradually decreases as $V+$ increases. After $V+=1.65V$, the system is completely balanced, all of the transistors in the current mirror pair are saturated, and $I(M_7)=I(M_8)=\frac{I(M_9)}{2}$ afterwards.

Table 6.4-6 The program to investigate the currents for Experiment 6.4-5

Experiment 6.4-6

```
.PROTECT
.OPTION POST
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op

VDD      VDD!      0      3.3V
VSS VSS!       0      0V

M1  1    1    VDD!    VDD!    PCH      W=50U       L=2U
M2  2    1    VDD!    VDD!    PCH      W=50U       L=2U
M3  3    3    1       VDD!    PCH      W=50U       L=2U
M4  4    3    2       VDD!    PCH      W=50U       L=2U
M5  3    VB7 5        VSS!         NCH         W=100U      L=2U
M6  4    VB8 6        VSS!         NCH         W=100U      L=2U
M7  5    Vi- 7        VSS!         NCH         W=100U      L=2U
M8  6    Vi+ 7        VSS!         NCH         W=100U      L=2U
M9  7    VB9 VSS!          VSS!          NCH          W=100U      L=2U

VIN+     Vi+       0     0v
VIN-     vi-       0     1.65v
VBIAS7   VB7 0     1.9V
VBIAS8   VB8 0     1.9V
VBIAS9   VB9 0     0.6V
VBIAS11 VB11      0          1.75V

Rm10     VDD!     10_1      0

.DC VIN+ 0 2.5V 0.01V
.PROBE I(M7) I(M8) I(M9)
.end
```

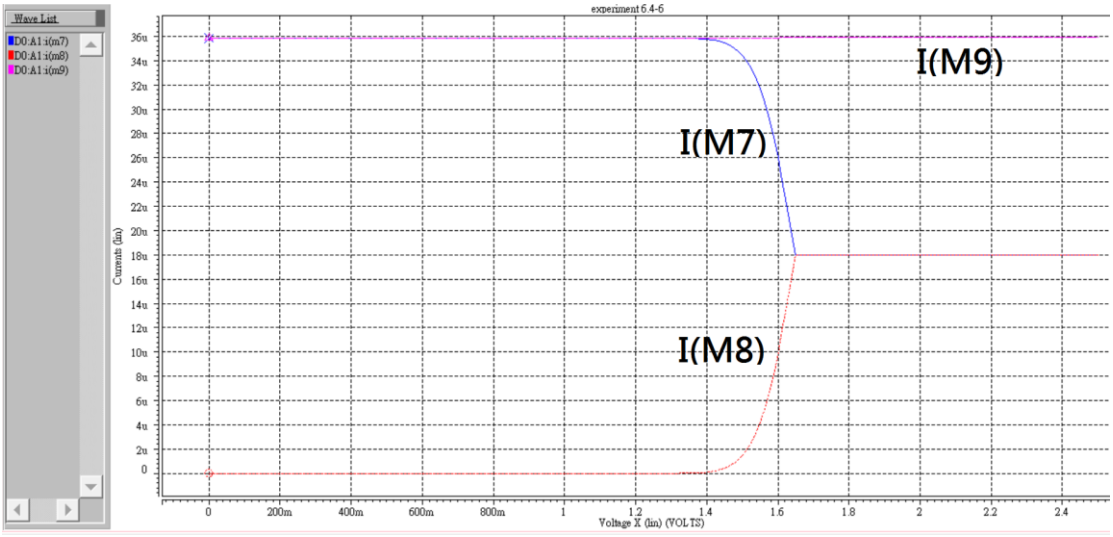


Fig. 6.4-6 The behavior of currents in the cascoded amplifier

We then investigated the behavior of the voltages. The program is in Table 6.4-7 and the results are in Fig. 6.4-7.

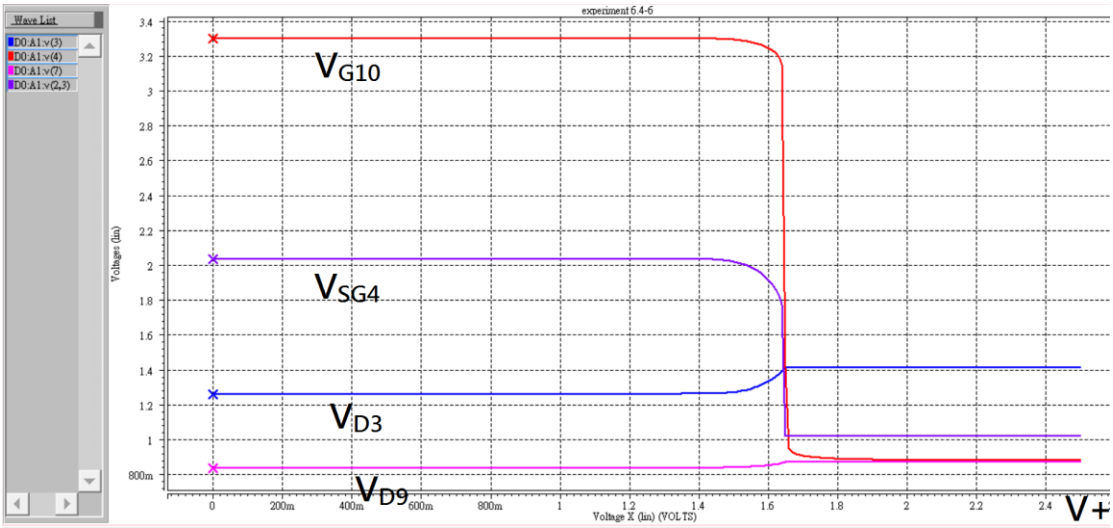


Fig. 6.4-7 The voltages in the cascaded differential amplifier

Before we present the observations, we must note an important point: Before $V+$ reaches 1.65V, the current mirror does not work because M_8 is cutoff and only the left side of the circuit is conducting. When $V+$ reaches 1.65V, the circuit is completely balanced. After $V+$ reaches 1.65V, the current mirror starts to work. The currents in both sides of the circuit are the same and kept as a constant. So will be the voltages.

The following observations are in order.

(1) V_{D3} is almost kept a constant all the way through. This can be explained by taking a look at $I(M_7)$. $I(M_7)$ is kept a constant except immediately before and after $V+=1.65V$. Since M_3 and M_1 are both diodes, their V_{SD}'s are kept constant. Therefore, V_{D3} is kept a almost constant

(2) V_{D9} is almost kept a constant all the way through. This can be explained by looking at $I(M_7)$ again. Before $V+$ reaches 1.65V, as seen from Fig. 6.4-6, as V_{i+} increases, $I(M_7)$ is kept a constant. $V_{GS7}=V_{G7}-V_{D7}=V_{G7}-V_{D9}$ must be a constant. Because V_{G7} is a constant, V_{G9} must be a constant.. We can use the above argument to the situation after $V+$ reaches 1.65V.

(3) $V_{G10}=V_{D4}$ is 3.3V when $V+$ is smaller than 1.65V. That is, it is very high when $V+$ is small. $V_{G10}=V_{D4}$ drops to be equal to V_{D3} when $V+=1.65V$. That $V_{G10}=V_{D4}=3.3V$ when $V+$ is smaller than 1.65V is due to the fact that $V_{SD4}=0$ when $V+$ is small as discussed in (5) above. That it drops to V_{D3} when $V+=1.65V$ because at this point, the circuit is completely balanced.

That $V_{G10}=V_{D4}$ is a constant after $V_{G10}=V_{D4}$ can be explained by using similar reasoning to explain why V_{D9} is a constant.

(4) V_{SG4} is a constant before $V+=1.5V$ because $V_{D4}=V_{G10}=3.3V$. Thus $V_{S4}=3.3V$ which is a constant. $V_{G4}=V_{G3}$ which is a constant. Therefore, V_{SG4} is a constant in this period. After $V+=1.5V$, $I(M_4)$ begins to rise and $V_{D4}=V_{G10}$ begins to drop. Yet, as seen in Fig. 6.4-7, V_{SD4} is kept a constant. Thus, V_{S4} falls. But, $I(M_3)$ falls. This causes $V_{G4}=V_{G3}$ to rise. The facts that V_{S4} falls and V_{G4} rises cause V_{SG4} to decrease.

It is easy to see why V_{SG4} is a constant after $V+=1.65V$

It will be a big puzzle for readers to observe that as V_{SG4} decreases for the period from $V_{i+}=1.5V$ to $V_{i+}=1.65V$, $I(M_4)$ actually increases. This is quite unusual because we would think that the current in a PMOS transistor will decrease if its V_{SG} decreases. To understand this, note that so far as M_4 is concerned, its load is M_8. V_{GS8} is increasing all the time. Therefore, we may say that the load of M_4, which is M_8, is decreasing. That is, two phenomenon are happening to M_4 simultaneously: (1) Its V_{SG} is decreasing and (2) its load is also decreasing. This situation is illustrated in Fig. 6.4-8. From Fig. 6.4-8, we can see that the current may increase as V_{SG} decreases because the load is also decreasing. Note that V_{SD} is extremely small, in fact 0, to start with.

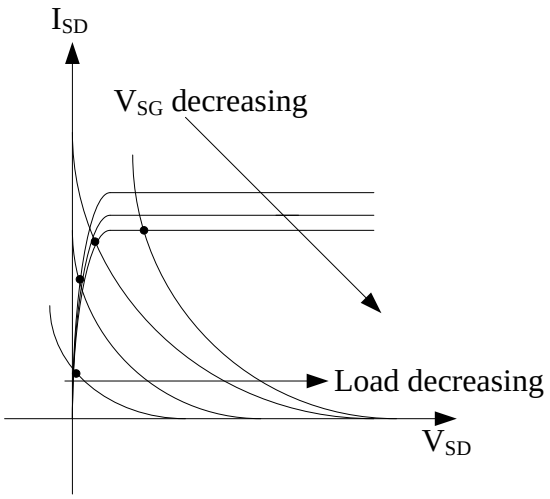


Fig. 6.4-8 An illustration of the decreasing of V_{SG4} and decreasing of it load.

Experiment 6.4-6 The I-V Curve of M_9 and Its Loads

As we introduced in Chapter 4, Vi+ is a load of M_9. We can expect that different Vi+'s produce different load curves. The program is in Table 6.4-7 and the result is in Fig. 6.4-9. As can be seen in Fig. 6.4-9, V_{DS9} almost does not change at all. This was explained in (2) in Experiment 6.4-5.

Table 6.4-7 The program for Experiment 6.4-6

```
Experiment 6.4-6
.PROTECT
.OPTION POST
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op

VDD     VDD!     0     3.3V
VSS VSS!     0     0V

M1  1    1    10_1     VDD!    PCH     W=50U      L=2U
M2  2    1    10_1     VDD!    PCH     W=50U      L=2U
M3  3    3    1        VDD!    PCH     W=50U      L=2U
M4  4    3    2        VDD!    PCH     W=50U      L=2U
M5  3    VB7  5        VSS!        NCH         W=100U     L=2U
M6  4    VB8  6        VSS!        NCH         W=100U     L=2U
M7  5    Vi-  7        VSS!        NCH         W=100U     L=2U
```

```
M8  6     Vi+  7          VSS!          NCH          W=100U       L=2U
M9  7     VB9 VSS!          VSS!          NCH          W=100U       L=2U

VIN+      Vi+        0     0
VIN-      vi-        0     1.65v
VBIAS7    VB7 0      1.9V
VBIAS8    VB8 0      1.9V
VBIAS9    VB9 0      0.6V
VBIAS11 VB11         0          1.75V
VDS9      7      VSS!       0

Rm10      VDD!     10_1       0

.DC VDS9 0 3.3v 0.1v SWEEP VIN+ 1 2.5V 0.2V
.PROBE I(M7) I(M8) I(M9) I(Rm10)
.end
```

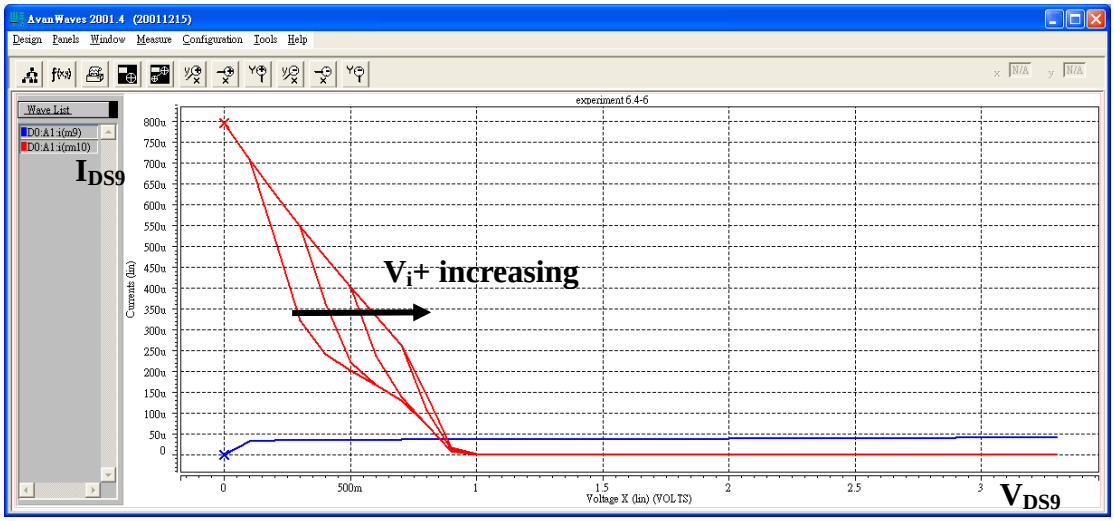


Fig. 6.4-9 I-V curve of M_9 and its load curves for different V_i+

Let us now try to explain another property of this cascaded amplifier. The input-output curve of this amplifier is very sharp as shown in Fig. 6.4-2 which is now displayed in Fig. 6.4-10. Our question is: How can the curve be so sharp?

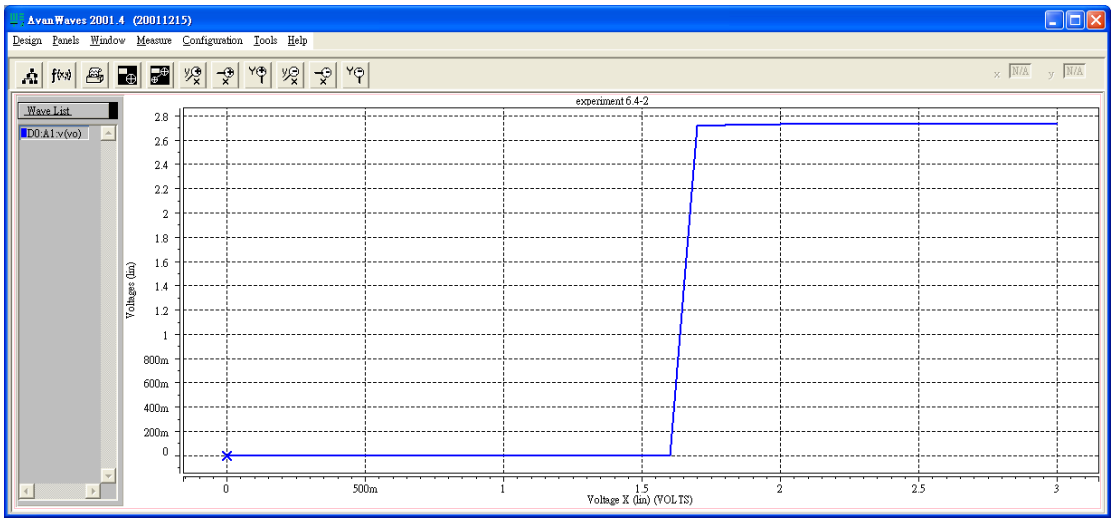


Fig. 6.4-10 The input-output curve of the cascade amplifier

To answer this question, we first display the circuit again as shown in Fig. 6.4-11.

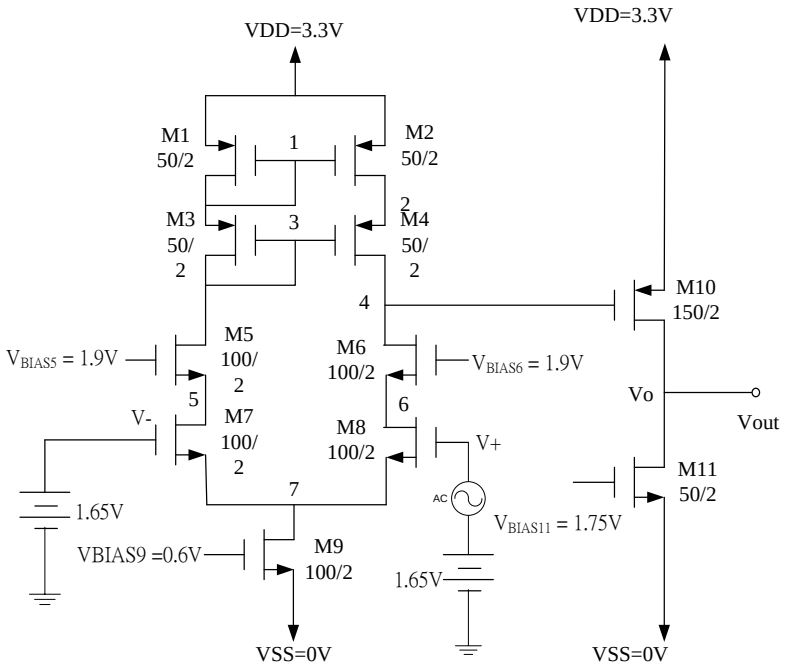


Fig. 6.4-11 The cascode amplifier circuit

Note that circuit consists of two stages. When we perform the DC input output analysis, we do not have a sharp output at Node 4, namely the drain of M_4. That is, the input to M_{10}, namely V_{G10}, is actually rather rounded, as shown in Fig. 6.4-7 which is now displayed as Fig. 6.4-12.

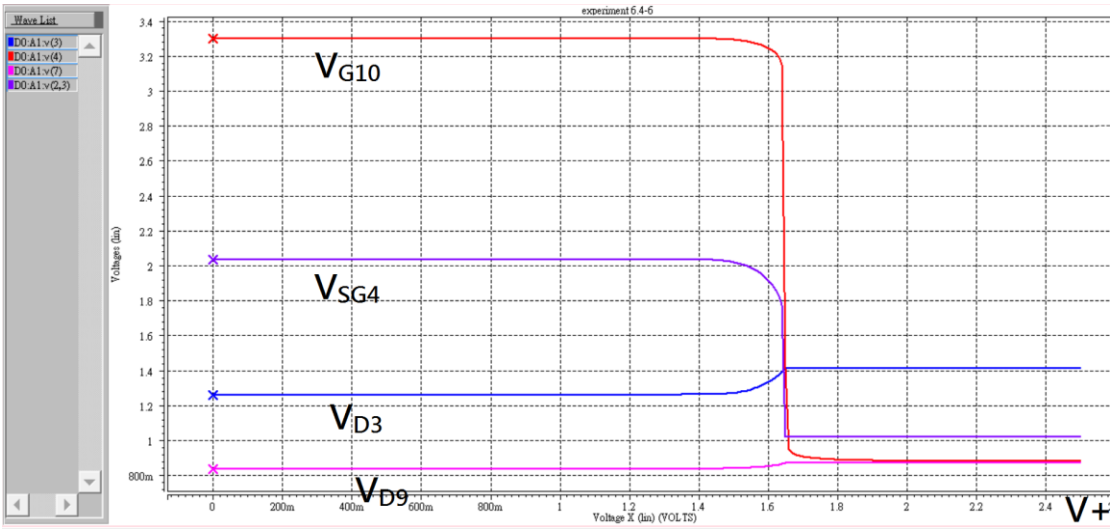


Fig. 6.4-12 The voltages in the cascaded differential amplifier

From Fig. 6.4-12, we can see that V_{G10}, the input of M_{10}, is not so sharp as the output voltage of M_{10}. This is due to the fact that the input of M_{10} is a very large one. So far as the DC analysis is concerned, the second stage amplifier, consisting of M_{10} and M_{11}, is an inverter. If the input of an inverter is a large one, the output is always a sharp one. In the following experiment, we shall confirm this fact.

Experiment 6.4-7 The Inverter Behavior of M_{10} and M_{11}

In this experiment, we give a sinusoidal input to M_{10}. This is a large signal. Thus the output is not sinusoidal at all. As can be seen, when the input rises gradually, the output falls sharply. This confirms what we stated before that the two transistors now act as an inverter. The program is shown in Table 6.4-8 and the result is in Fig. 6.4-13.

Table 6.4-8 The program for Experiment 6.4-7

```
Experiment 0331
.PROTECT
.OPTION POST
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op

VDD     VDD!     0     3.3V
VSS VSS!     0     0V
```

```
M10 Vo   4     10_1      VDD!     PCH      W=150U      L=2U
M11 Vo   VB11 VSS!       VSS!     NCH      W=50U       L=2U

VIN+     4       0  sin(1.4V 0.5V 10k)
VBIAS11 VB11      0          1.75V

Rm10     VDD!    10_1      0
*VSD10  VDD!     Vo   0

*.DC     VSD10   0     3.3v 0.1v
*.probe  I(Rm10)  I(M11)
.tran 0.1us 0.5ms
.end
```

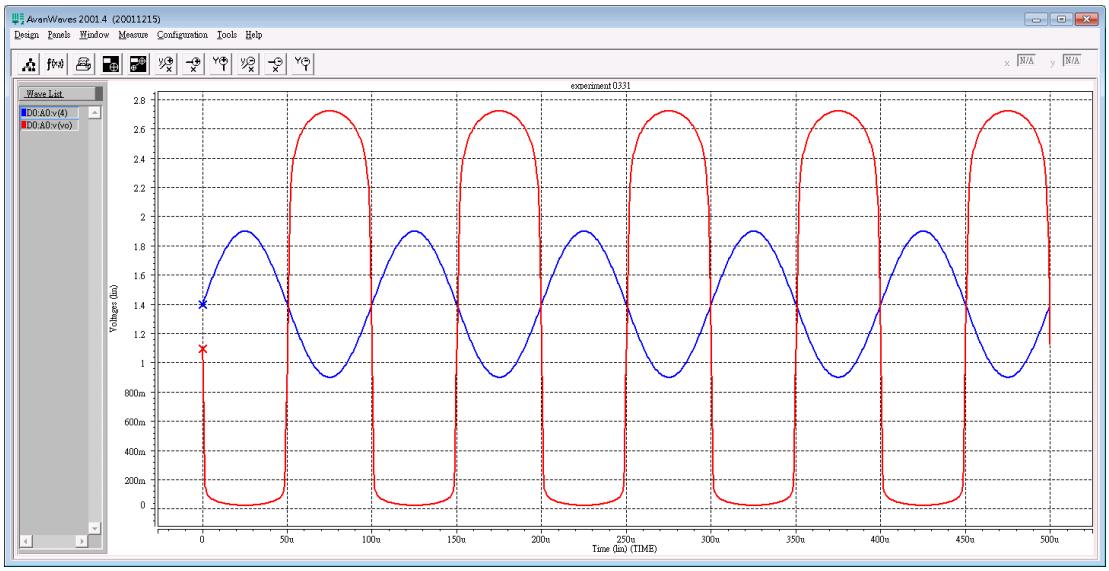


Fig. 6.4-13 The result of Experiment 6.4-7

There is a point which we should pay attention to. Consider the circuit which appeared in Fig. 4.3-7. To facilitate discussion, we redisplay Fig. 4.3-7 as Fig. 6.4-14..

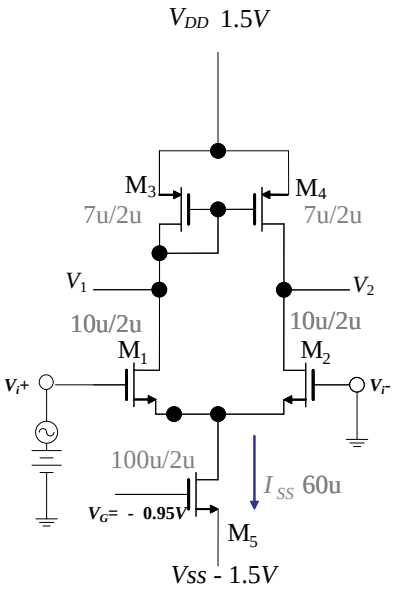


Fig. 6.4-14 The redisplay of Fig. 4.3-7

The currents of the circuit were in Fig. 4.4-8 and are now redisplayed in Fig. 6.4-15.

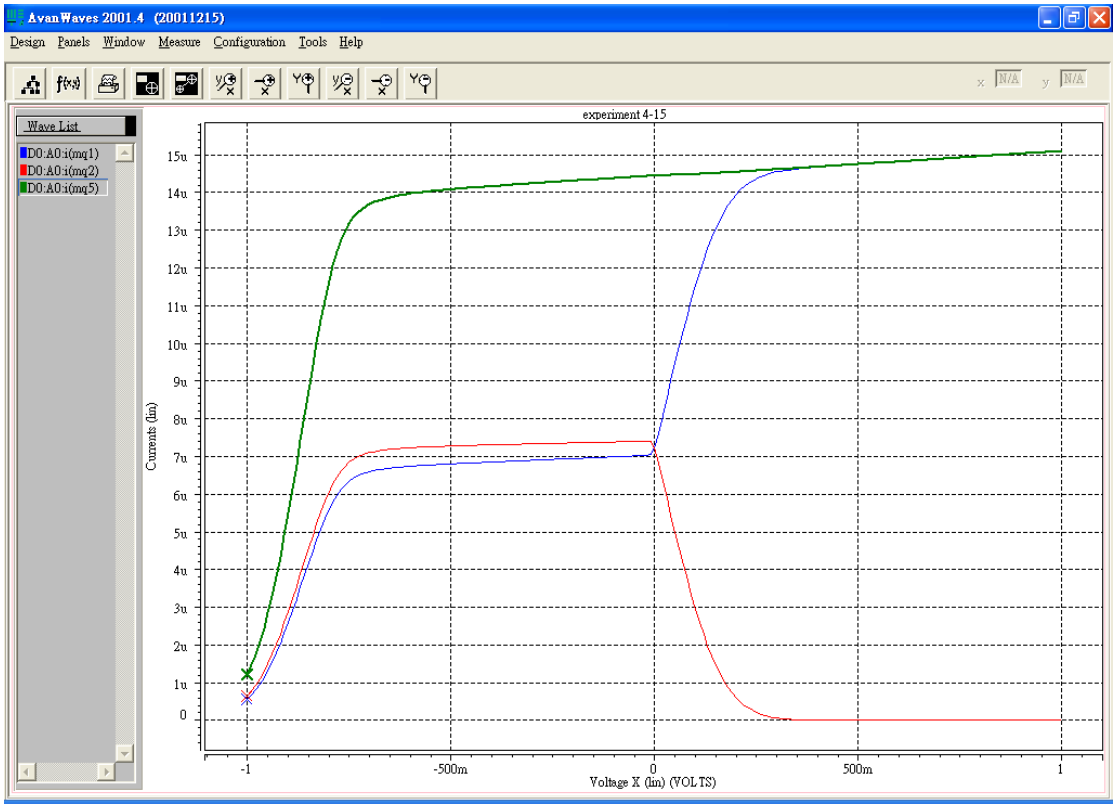


Fig. 6.4-15 Redisplay of Fig. 4.4-8

Now, let us further consider the cascoded differential amplifier discussed in this chapter. Fig. 6.4-16 shows the circuit.

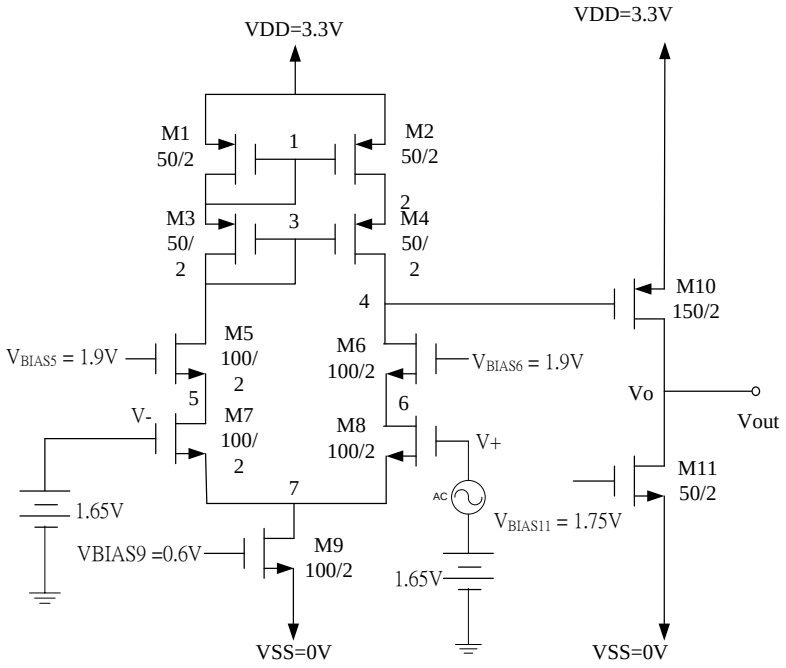


Fig. 6.4-16 The cacoded differential amplifier introduced in this chapter.

The currents of this cicruit was in Fig. 6.4-6. We redisplay it in Fig. 6.4-17

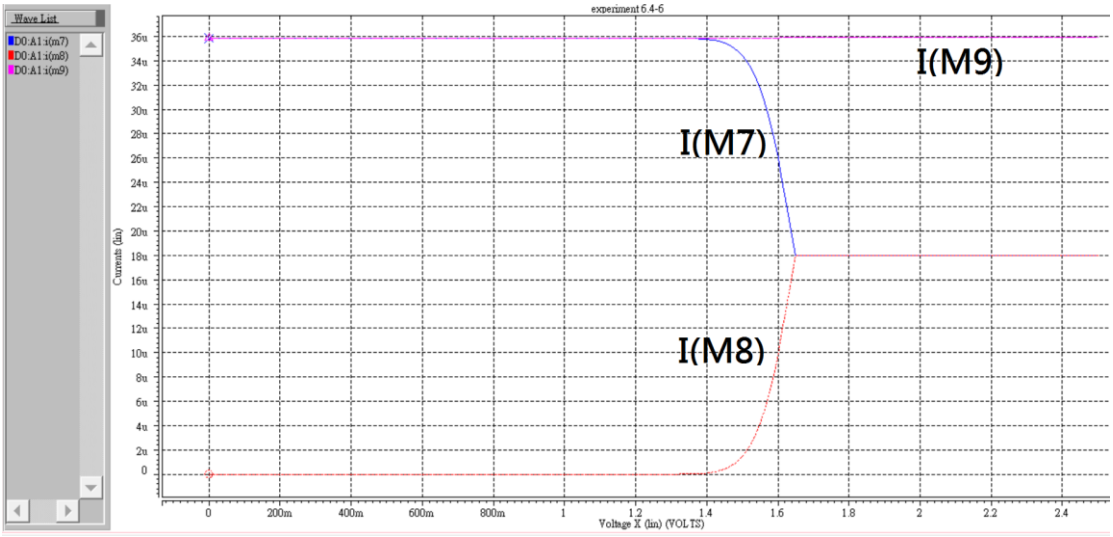


Fig. 6.4-17 A redisplay of Fig. 6.4-6

The two differential amplifiers are qute similar. Yet the behaviour of their currents are entirely different as can be seen from Fig. 6.4-15 and Fig. 6.4-17. This puzzle is now explained.

Consider the amplifier in Fig. 6.4-14. Note that in this case, the changing voltage V+ is applied to M_1. If V+ is low, $I(M_1)$ will be 0. Therefore, $I(M_3)$ will also be cutoff. Because M_3 is a diode, $V_{SD3}=V_{SG3}=0$. This makes M_4 being cutoff which means that $I(M_2)=0$. Consequently, we can see from From Fig. 6.6-15 that both $I(M_1)$ and $I(M_2)$ are almost 0 when V+ is small.

Now, consider the amplifier in Fig. 6.4-16. In this case, V+ is applied to M8 which is not connected any diode. If V+ is low, it does make $I(M_8)$ to $I(M_2)$ all being 0. But it will not cause $I(M_1)$ being 0. That is, there can be current in M_7 although no current in M_8 as shown in Fig. 6.4-17..

We conclude that if we use the circuit in Fig. 6.4-16 and apply the changing voltage to M_7, the currents will be exactly the same as that in Fig. 6.4-15.

Experiment 6.4-8 The Changing Voltage is Applied to M7, Instead of M8

In this experiment, the gate voltage of M_7 is changing while that of M_8 is fixed to be 1.65V. The program is in Table 6.4-9 and the result is in Fig. 6.4-18. We can see that our conclude is correct.

Table 6.4-9 Program for Experiment 6.4-8

```
Experiment 6.4-8
.PROTECT
.LIB "C:\mm0355v.l" TT
.UNPROTECT
.op
.OPTION POST

VDD     VDD!     0     3.3V
VSS VSS!     0     0V

M1  1   1   VDD!   VDD!   PCH     W=50U      L=2U
M2  2   1   VDD!   VDD!   PCH     W=50U      L=2U
M3  3   3   1      VDD!   PCH     W=50U      L=2U
M4  4   3   2      VDD!   PCH     W=50U      L=2U
M5  3   VB7 5      VSS!       NCH         W=100U     L=2U
M6  4   VB8 6      VSS!       NCH         W=100U     L=2U
```

```
M7  5    Vi-  7      VSS!       NCH        W=100U     L=2U
M8  6    Vi+  7      VSS!       NCH        W=100U     L=2U
M9  7    VB9 VSS!       VSS!       NCH        W=100U     L=2U

VIN+     Vi+      0    1.65v
VIN-     vi-      0    1.65v
VBIAS7   VB7 0    1.9V
VBIAS8   VB8 0    1.9V
VBIAS9   VB9 0    0.6V
VBIAS11  VB11     0         1.75V

Rm10     VDD!     10_1      0

.DC VIN- 0 2.5V 0.01V
.PROBE I(M8) I(M9) I(M7)
.end
```

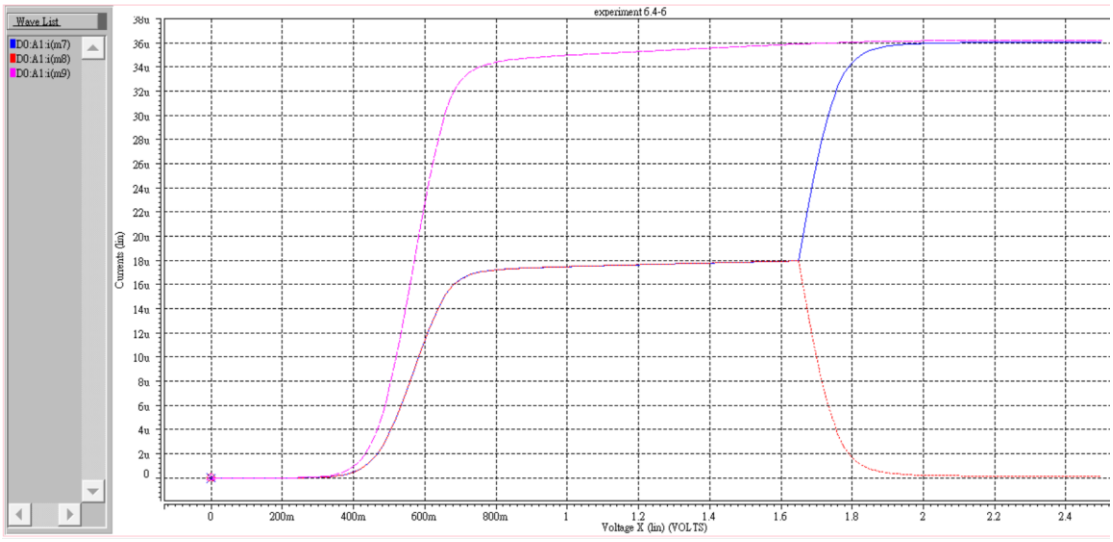


Fig. 6.4-18 The result of Experiment 6.4-8